Reliability Studies of Ultra-Small Copper-Plated Through-Package-Vias in Ultra-Thin Glass Interposers

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Kaya Demir

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Reliability Studies of Ultra-Small Copper-Plated Through-package-vias in Ultra-Thin Glass Interposers

Approved by:

Dr. Rao R. Tummala, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Ajeet Rohatgi
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Oliver Brand
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. P. Markondeya Raj
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Levent Degertekin
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Raghuram Pucha
School of Mechanical Engineering
Georgia Institute of Technology

Date Approved: 10/31/2016

To my mom, Fatma Sema Demir

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TABLE OF CONTENTS

Page

LIST OF TABLES

Page

LIST OF FIGURES

Page

SUMMARY

The escalating demand for higher bandwidth with high interconnection densities and ultra-short interconnections between components has been a key driver for package innovations. One such application is the high bandwidth between logic and memory devices in a processor package. Other examples include mm wave packages with lowest parasitics from ultra-short interconnections between various active and passive components. Innovative 3D interposers and packages are emerging as a promising solution to achieve such high bandwidth with low power and low cost. Emerging panel fan-out package architectures are also driven by high via densities between the embedded die and the rest of the system components. A key element of these is a thin substrate with ultra-small through-package-vias (TPVs) to vertically connect the components on one side of the interposer to the other side.

The current approach for 3D packaging is primarily based on organic or silicon interposers. However, organic interposers face several challenges due to their poor dimensional stability, limiting the wiring and I/O density. Silicon interposers made with back-end-of-line (BEOL) wafer processes can achieve the required wiring and I/O density, but they are not cost effective due to expensive through-silicon-via processes, and they exhibit higher electrical loss due to the semiconducting nature of the Si substrate.

Glass is emerging as a superior and low-cost alternative to organic and silicon interposers due to its high dimensional stability enabling high density I/O and high electrical resistivity leading to low electrical loss. However, glass is a brittle material. Inherent glass defects, especially on the bare glass surfaces, lead to poor mechanical strength that can be further degraded by defects formed during via drilling. Furthermore, the coefficient of thermal expansion (CTE) mismatch between copper and glass induces thermomechanical stresses in

TPVs which may lead to various reliability issues such as cohesive cracking and interfacial separation. Reliability of copper-plated through-package-vias in glass interposers forms the fundamental focus of this research.

The objective of the research is to model and design copper-plated through-package-vias, leading to fabrication of test vehicles for characterization of defects, and validation of models by demonstration of reliability through accelerated lifetime testing. To meet these objectives, this study focusses on four main tasks, a) mechanical modeling and design of TPVs in glass, b) fabrication of test vehicles for reliability characterization, c) reliability characterization of TPVs, and d) analysis of failures to validate the models.

Extensive parametric modeling of TPVs is performed to provide design guidelines for reliable TPVs. Three glass package structures are investigated: polymer-laminated glass, bare glass, and TPVs with polymer-liner. Test-vehicles with all the three structures are designed and fabricated. Various TPV formation approaches such as excimer, UV, CO_2 lasers and electrical discharge techniques were utilized to fabricate the test-vehicles. Quality of TPVs formed with each of these methods are analyzed through cross-section SEM imaging to identify characteristic defect sizes and geometries corresponding to each method. Thermo-mechanical reliability tests and failure analyses are performed to study TPV reliability. Micro Raman spectroscopy was used to measure stresses in glass packages for the first time. The results from test-vehicle characterization are consistent with the modeling predictions, thus providing a valid set of design rules for manufacturing of reliable TPVs. This thesis, thus, reports the first comprehensive study on reliability of copper-plated ultra-small through-package-vias in ultra-thin glass interposers.

CHAPTER 1

INTRODUCTION

1.1 Strategic Need

The evolution of ultra-miniaturized portable systems such as smartphones with the proliferation of graphics, games and other data-centric needs is expected to accelerate the demand for ever increasing memory to-logic bandwidth [1]. This escalating bandwidth need for mobile products is illustrated in Figure 1.1. As seen from this figure, the memory bandwidth is projected to exceed 30 GB/s for hand-held products, well beyond the capabilities of current technologies [2].

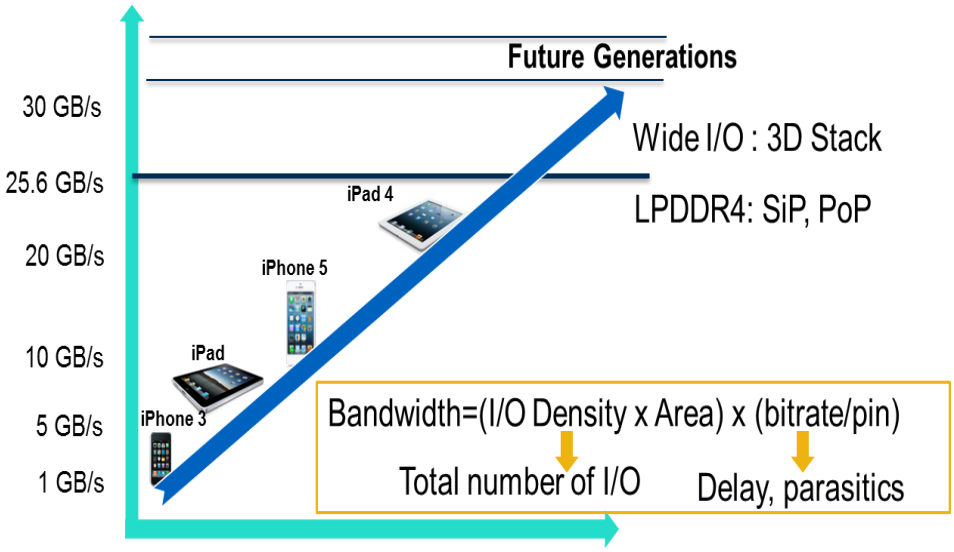


Figure 1.1. Demand for high bandwidth in mobile applications

In addition, these bandwidth requirements need to be met with lower power and larger memory at lower cost. These system needs are typically limited by the I/O density and interconnection length. One approach to address this rising demand is traditional transistor scaling with system-on-chip (SOC). In the past three decades, the microelectronics industry has

largely been driven by Moore's law to continuously increase device density and circuit speed. This led to reducing the transistor node to 14 nm. However, beyond 14nm transistor node, the SOC implementation is expected to reach performance and cost barriers. This escalating cost and performance challenges with advanced transistor nodes has fueled a growing interest in advancing packaging technologies other than continued down-scaling of microelectronic devices on a 2-dimensional plane. Therefore, to minimize interconnection parasitics and to meet the bandwidth requirements, traditional 2D multi-chip packages such as multichip modules with large interconnect lengths and low I/O density are, therefore, evolving into 2.5D and 3D ICs with shorter interconnect lengths and higher I/O density, as shown in Figure 1.2 [2]. These approaches offer at least 3 major advantages: 1) better electrical performance; 2) lower power consumption; 3) higher device density in smaller package form factors. Replacing horizontal connections with shorter vertical interconnections can simultaneously reduce signal time and power needed for data transmission. Furthermore, higher device density and smaller packaging size can eventually reduce manufacturing cost.

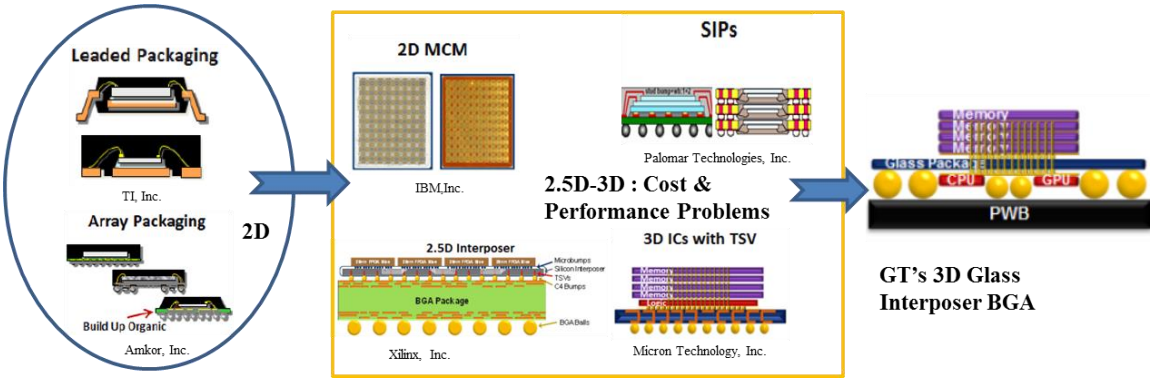


Figure 1.2. Evolution of electronic packages from 2D to 3D for high bandwidth (Courtesy of Prof. Tummala)

Current 3D approaches based on wire-bonded die stacking and Package Stacking (or Package on Package) has enabled bus speeds up to ~1 GHz with about 100 channels, limiting their bandwidth to approximately 2 GB/s. To further improve the data-rates and power efficiencies, there is a compelling need to vertically package multiple ICs and interconnect the ICs within the IC footprint to reduce the global interconnection length, thus leading to improved performance and bandwidth. Several approaches are being pursued for such vertical integration of ICs, one of which is based on stacked ICs with Through-Silicon-Vias (TSVs) as 3D ICs [3]. This approach can achieve high bandwidth for two reasons: short interconnection length and the sheer number of parallel channels that they can support. However, numerous challenges remain with this approach, including cost, thermal management, testability, scalability and system integration.

Another promising approach to achieve the same attributes is proposed by Georgia Tech using 3D interposers, not with TSVs in logic ICs but with TPVs in the package substrate, and assembling logic and memory ICs on both sides of ultra-thin interposer substrates, which are then assembled onto the printed circuit board without organic BGA packages in-between. These 3D interposers, called interposer BGAs, are used to vertically interconnect multiple ICs through assembly on both sides of the interposer, and in addition are also used to connect multiple ICs on the same side, in the so-called side-by-side configuration, referred to as 2.5D assembly. This technology, which is called system-on-package (SOP), is scalable, testable and enables ultra-short interconnection length and ultra-high interconnection density between logic and memory ICs just like with TSVs. Furthermore, SOP technology can eliminate the dimensional gap between ICs, packages and printed-circuit-boards (PCBs), thus leading to high system

functionality in smallest system size. This technology can also be extended RF, photonic and other sub-systems. The schematic cross-section drawing of SOP is shown in Figure 1.3.

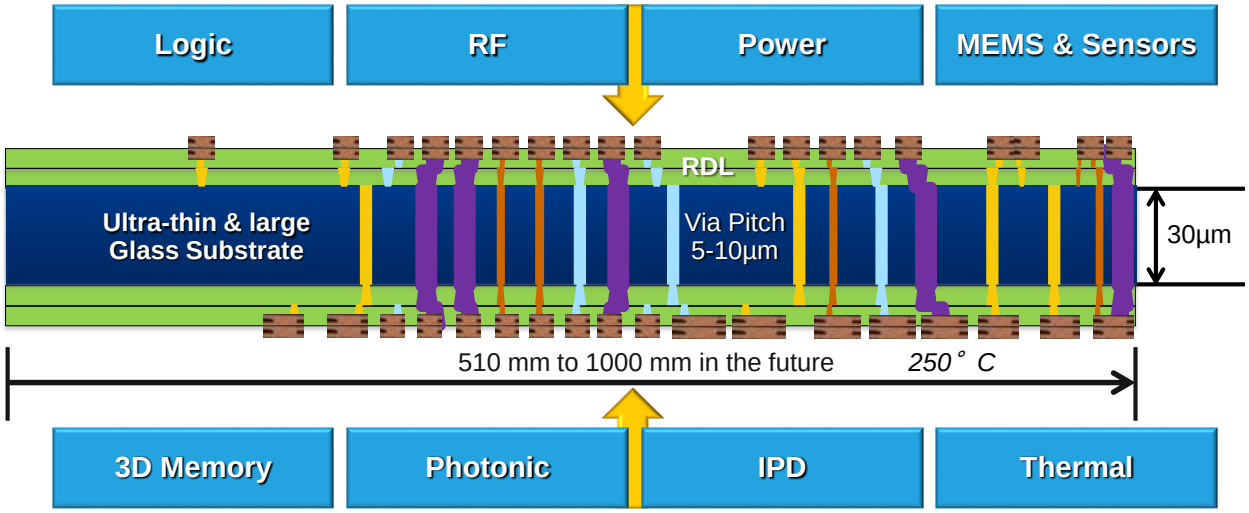


Figure 1.3. SOP concept for 3D system integration (Courtesy of Prof. Rao Tummala)

However, in both 3D and 2.5D configurations, interposer materials should have ideal electrical, thermal and mechanical properties, in addition to low cost manufacturing processes for through-vias, called through-package vias (TPV) and multilayer redistribution layers (RDL). Various substrate candidates have been considered for interposer applications. These include organic, ceramic, metal, single crystal silicon, polysilicon or glass. Figure 1.4 compares these package materials against ideal properties and their estimated processing costs at 25 μm I/O pitch.

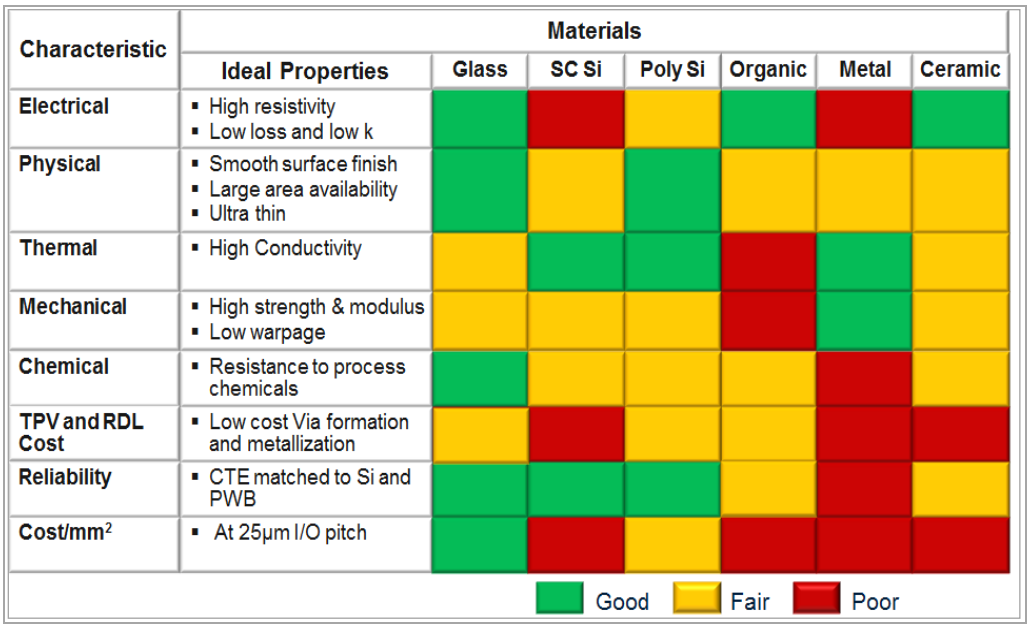


Figure 1.4. Comparison of various package materials for interposer applications (Courtesy of Prof. Rao Tummala).

Of these candidate materials for interposer BGAs, organic laminates are preferred because of their low cost and existing manufacturing infrastructure. However, they are limited in fine-pitch I/O capability due to their poor dimensional stability during fabrication processes, requiring large capture pads for layer-to-layer via registration. Therefore, organic interposers face several challenges below 40 µm bump pitch. High warpage is another predominant feature of organic packages that brings additional challenges in lithography for fine-line formation and assembly, and thus limits the maximum I/O count per area that organic materials can support [4].

To address these shortcomings, silicon interposers have been, and continue to be developed, manufactured and used in special high-performance applications, such as network servers, CPU and GPU servers. Manufacturing infrastructure for silicon interposers already exists because they are fabricated with standard back-end-of-line (BEOL) wafer processes to

achieve the required wiring and I/O density [5]. However, silicon interposers suffer from two major disadvantages: 1) high fabrication cost and 2) poor electrical performance. High fabrication cost is attributed to the limited number of interposers that yield from a 200-300 mm silicon wafer. In addition, the high cost comes from expensive processes to form TSVs, such as depositing insulating liners and single-side redistribution layers using back-end-of-the-line (BEOL) processes. Poor electrical performance is a result of electrical loss due to the semi-conductive nature of silicon, in spite of the thin SiO_2 dielectric layer. Thin SiO_2 layer around TSV wall is not sufficient to prevent electromagnetic waves from penetrating into the semi conductive silicon, thus leading to electrical loss. Furthermore, thermally- induced stresses on thin insulation layer can also result in reliability problems, and lead to cracking in the dielectric layer, current leakage into silicon and finally signal degradation.

1.2 Glass as an ideal candidate for 3D interposers and packages

To address the challenges associated with silicon and organic interposers, glass was proposed and is being developed by Georgia Tech and its 50 industry consortium partners, since 2010. Glass appears to be an ideal interposer material due to the following reasons: 1) Dimensional stability, 2.)High modulus for low warpage compared to organic packages, 3.)Variable CTE for optimized off-chip and board-level interconnections, 4) Excellent surface smoothness (1-2 nm roughness) enabling fine-line formation, 5) High electrical resistivity and low electrical loss, similar to ceramics, eliminating the requirement of having to insulate with liners in via walls, 6) Availability in ultra-thin (30-100μm) form-factors enabling ultra-short interconnections with double-side assembly, and 7) Availability in large panels leading to potentially low manufacturing cost [6]. These advantages of glass are summarized in Figure 1.5.

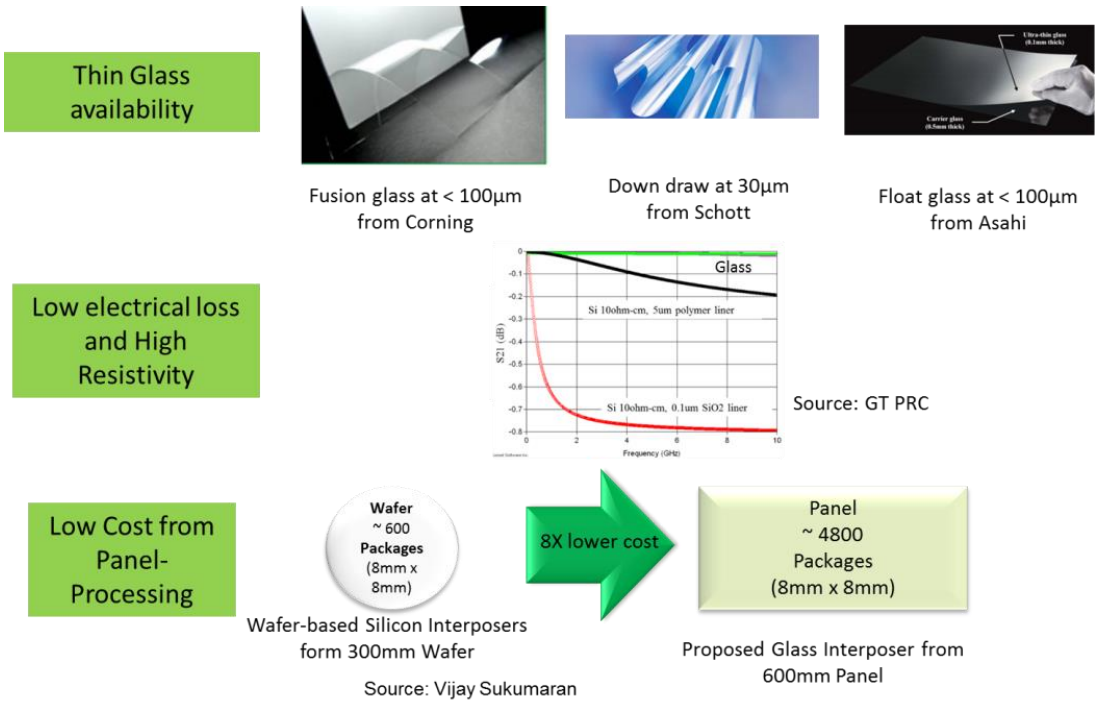
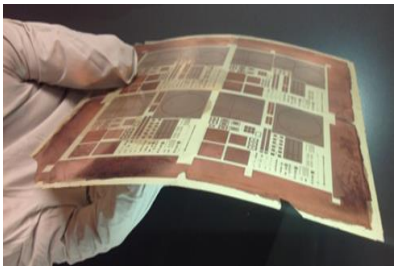
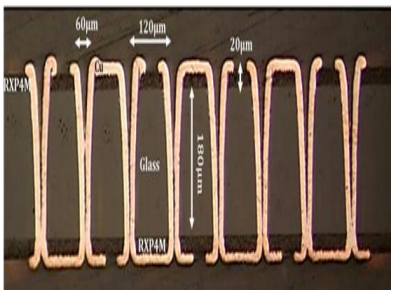


Figure 1.5. Advantages of glass as an interposer material (Dr. Vijay Sukumaran)

Several advances in glass-based interposers and packages have been demonstrated by the Georgia Tech team. Challenges in forming TPVs in glass have been solved recently to some level of speed by using ArF excimer laser and electrical discharge processes that enable drilling of more than 1000 holes in few seconds [6, 7]. Metallization of high aspect ratio TPVs was achieved by electroless and electrolytic copper plating and handling of ultra-thin glass was achieved by polymer lamination. Glass interposers were demonstrated to be electrically superior, compared to wafer-based silicon interposers [8]. Superior electrical performance of RF passives, integrated RF modules, and high bandwidth transmission lines on glass interposers were demonstrated. [9]. Panel-scale glass interposer and package fabrication processes described in these previous studies promise significant cost benefits [10]. Some of these advancements are illustrated on Figure 1.6.



(a)



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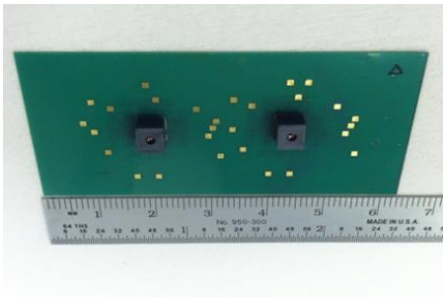

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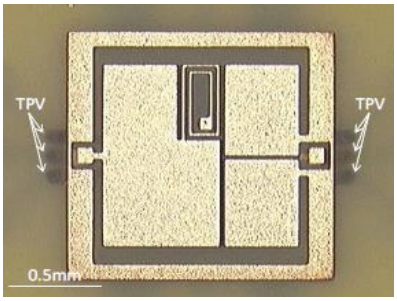


(d)

Figure 1.6. (a) Fabricated 6" glass panel with 30 µm thickness , (b) Metalized TPVs with aspect ratio of 3, (c) Camera module and (d) Low-Pass Filter on glass (Courtesy of GT PRC)

1.3 Fundamental Challenges with TPVs in Glass Interposers

In spite of the advances described in Section 1.2, reliability of Cu-TPVs remains a major concern in realizing the glass-based 3D interposers and packages. Glass is an almost perfectly elastic material. In other words, when a mechanical load is applied to glass, it will not suffer any permanent or plastic deformation, but will always return to its original dimensions irrespective of the number of times it is deformed. However; glass is a brittle material that means it can fail at

elastic strains as low as 0.2% as illustrated in Figure 1.7 [11]. Glass gets even more fragile in contact with water.

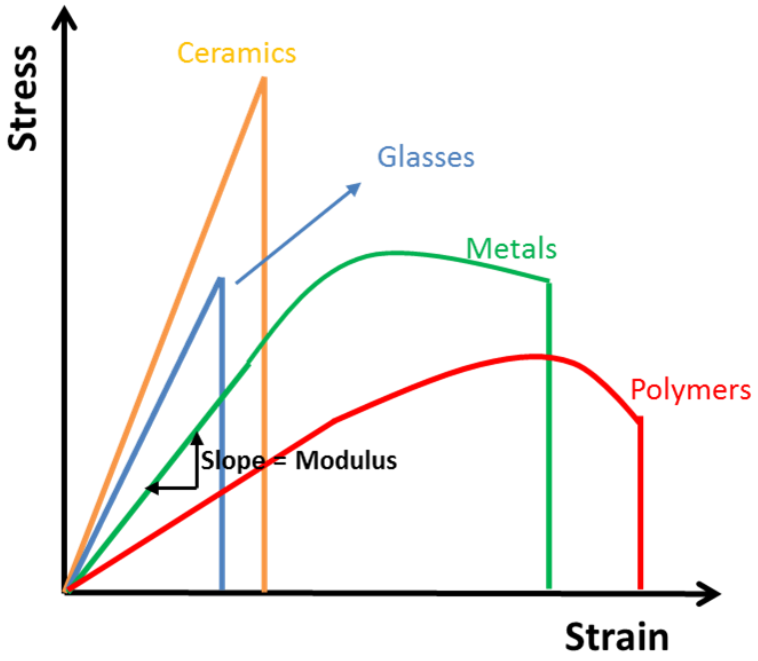


Figure 1.7. Stress-Strain graph of glass compared to metals, ceramics and polymers

Glass is an inherently strong material, especially against compression but weaker against tension. Strength of a freshly drawn glass is very high due to its pristine surface and absence of flaws and defects; however, surface defects are introduced during subsequent processing steps that significantly lower the strength [12]. Critical stress value for brittle fracture is related to the defect size according to the Griffith's equation shown in Figure 1.8. Inherent glass defects, especially on the bare glass surfaces, lead to poor mechanical strength that can be further degraded by defects formed during via drilling. Defects and through-via holes may act as stress concentrators that can become the initiation points for cracks, leading to catastrophic failures.

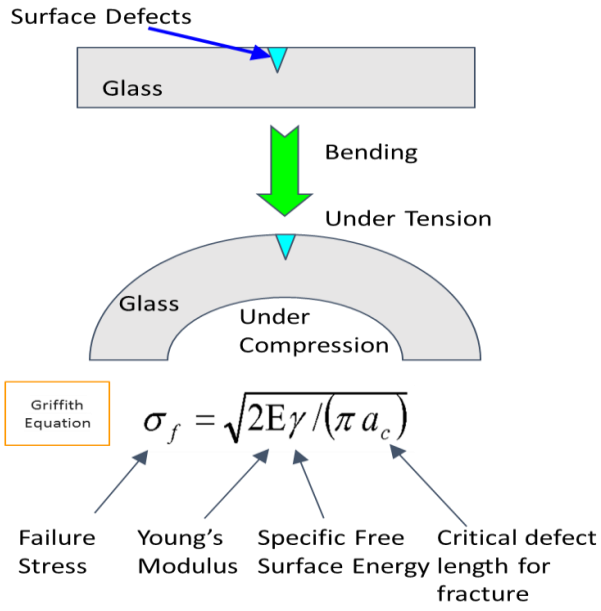


Figure 1.8. Griffith criterion for fracture of glass substrates

Thinner substrates are preferred to reduce the module thickness and also reduce the interconnection length for lower parasitics in ultra-miniaturized 3D electronic packages. With decreasing thickness, glass becomes more flexible and can bend to smaller radii of curvatures with lower bending stress as illustrated in Figure 1.9 [13]. Fracture toughness of glass does not change with thickness; however, with decreasing thickness, it becomes easier to induce stresses that can break the glass during handling and fabrication processes. Glass thickness is also limited by microscopic defect sizes on glass surfaces that limit its fracture stress.

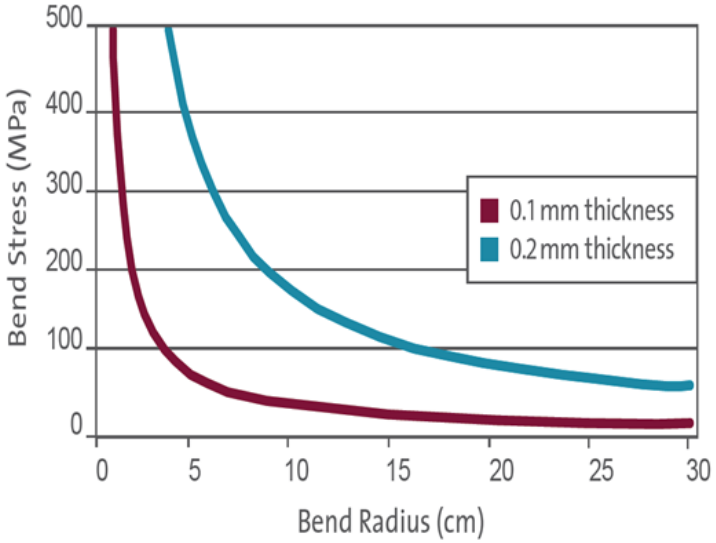


Figure 1.9. Variation of stress with bend radius for 2 different glass substrate thicknesses

The CTE mismatch between Cu with CTE of 17ppm/^{o}C and glass with CTE of 3-9 ppm/^{o}C is the major source of thermo-mechanical stresses in Cu-TPVs. During thermal cycling, this mismatch generates high thermal stresses in the glass surrounding the Cu TPVs, as well as strain deformations in the copper, as shown in Figure 1.10. These stresses may lead to various reliability issues, such as cohesive cracking and interfacial separation.

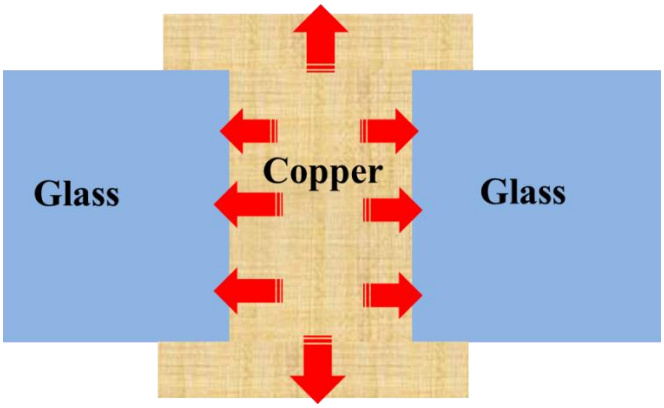


Figure 1.10. CTE mismatch- induced thermal load on glass at temperatures higher than the stress-free temperature.

These thermal stresses are further amplified in the presence of defects on TPV walls and corners, and eventually lead to crack formation in glass. The allowable defect sizes from TPV formation processes is limited by the CTE-induced stresses. When the system is heated, higher expansion of copper compared to glass creates radial compression and circumferential tension in glass. On the other hand at cold extreme temperatures, contraction of copper induces radial tension and circumferential compression in glass. For fully-filled vias, the maximum radial (σ_r) and circumferential (σ_θ) stresses in the surrounding glass can be approximated using a 2-D analytic solution [14]. This approximation is valid at locations far away from the ends of the TPV:

$$\sigma_r = -\sigma_\theta = -\frac{\mathrm{B}\,\Delta\alpha\,\Delta\mathrm{T}}{2} \tag{1.1}$$

Where B is the biaxial modulus of Glass (100 GPa), $\Delta\alpha$ is the CTE mismatch between Cu and glass (14ppm/^{o}C), and ΔT is thermal load. A simplified risk assessment can be made using this 2-D analytic solution. According to Equation 1.1, for a thermal load of ΔT=260^{o}C during reflow, a radial compression and tangential tension stress of approximately 180 MPa is induced at the Cu/Glass interface. Assuming fracture toughness of glass as 0.5 MPa m$^{1/2}$ and using an approximate stress intensity factor equation for edge defects under uniform tension [15]:

$$K_I = \sigma\sqrt{\pi a} \times 1.12 \tag{1.2}$$

where K_I, σ and a are fracture toughness, critical stress and defect size respectively, it is possible to estimate the critical defect size for fracture. Assuming a radial edge crack and neglecting the reduction of stress with distance from Cu/Glass interface, critical defect size is approximately estimated as 2 µm. In addition, fracture toughness of glass reduces with interaction with water [16], and also possibly by TPV formation processes. Furthermore, stress values are much higher

around the ends of TPV surfaces. Therefore, via formation processes should be optimized for minimum defects and TPV materials and geometries should be designed for reliability.

Additional stresses arise from glass-handling during fabrication. Polymer lamination onto glass eases both glass handling and stresses induced from CTE mismatch [17]. This approach has at least 5 advantages: 1.) Less mechanical impact on glass during handling. 2.) Easier handling of thin glass as the polymer fills ultra-small defects on glass surfaces, thus increasing its strength. 3.) Polymers also slows down moisture adsorption onto glass surfaces, thus minimizing the weakening effects from interaction of water molecules with glass. 4.) Lower induced stress by acting as a stress-buffer layer. High elongation and low-modulus polymer films are effective in relieving stress by up to a factor of 3X. 5) Easier metallization of polymer surfaces compared to smooth glass surfaces [18].

In spite of the benefits with polymer-laminated glass, there are many other advantages to directly process bare glass with pre-processed through-vias: 1) More via formation options to reach smaller TPV diameter at finer pitch 2) Better RF performance due to lower dielectric loss of glass compared to traditional polymer dielectrics 3) Reduced number of fabrication steps and also the total thickness of interposer. Therefore, reliability of Cu-plated TPVs in bare glass is also of significant interest.

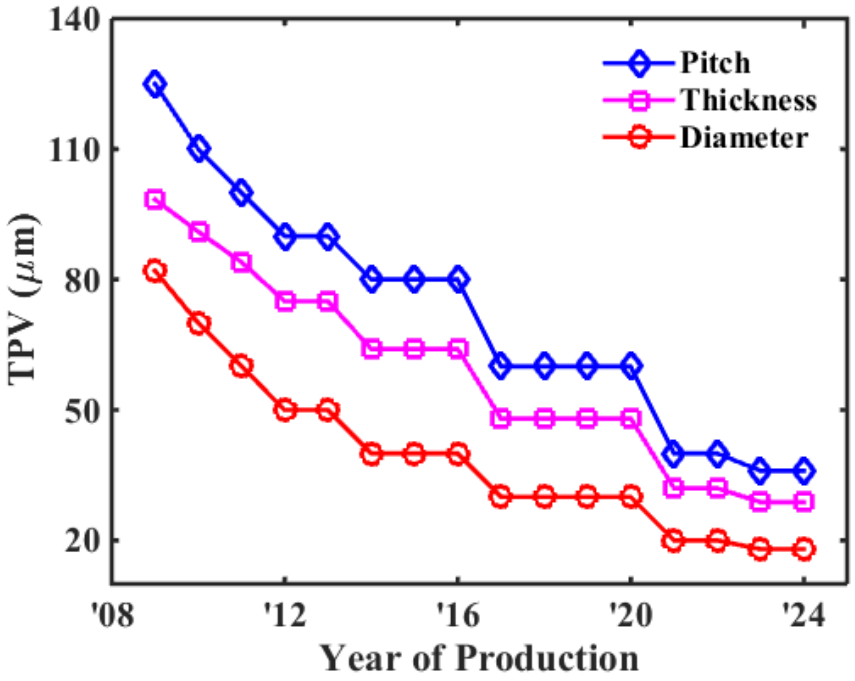


Figure 1.11. Trend for through-via diameter, pitch and glass thickness (Courtesy of ITRS)

The need for higher bandwidth will continue to scale-down the TPV pitch, as shown in Figure 1.11. In addition, glass thicknesses and via-hole diameters will continue to scale down in order to improve I/O density and shorten interconnect length, further aggravating the reliability concerns. Additionally, the probability of failure of a package increases as the number of TPVs increase in high-density packages. Therefore, a comprehensive approach starting from TPV modeling, design, leading to process development and fabrication is required to realize reliable TPV structures. The real benefits of ultra-thin glass interposers are, however, seen with double side or 3D assembly of active and passive components on glass. Assembled components on both sides affect the global and local thermal CTE mismatches and introduce additional thermomechanical stresses on TPVs. Therefore, reliability of Cu-plated TPVs in 3D assembly also needs to be investigated.

The objective of the proposed research is to model and design copper-plated through-package-vias, leading to fabrication of test vehicles for characterization of defects, and validation of models by demonstration of reliability through accelerated lifetime testing. The specific research objectives, prior art, proposed approach and challenges are summarized in Table 1.1.

Table 1.1: Research objectives, Prior art, challenges and tasks

1. Objectives	2.Prior Art	3. Challenges	4.Tasks
• Low TPV stresses and high fatigue life compared to organic or silicon packages	• Modeling of stresses in through-silicon-vias	• Brittleness of glass • Large CTE mismatch between glass and copper • Large variation in process and design parameters	Mechanical modeling of TPVs • Parametric analysis of TPV stresses; • Fracture mechanics analysis
• Evolve design guidelines from the modeling • Design test-structures to characterize large number of TPVs	• Design guidelines for fine-pitch vias in Si	• Design for both coarse and fine-pitch TPV failures, and double side assembly • Sensitivity of high-frequency behavior to defects	Design of test vehicles for reliability characterization • Design TPVs with bare and polymer-laminated glass • Design for testing in both DC and RF domains
• Process development and optimization of TPVs • Fabrication of test-vehicles with various TPV dimensions, materials and TPV formation options	• Polymer-laminated glass (100 microns) and conformal plated TPV	• Handling bare glass • Metallization of glass with adequate adhesion • Impact of assembly on TPV strains	Fabrication of test vehicles for reliability characterization • Polymer-laminated and bare glass (<100 μm); • Conformal and fully-filled TPVs • 3D Die Assembly
• Correlate the defects to formation methods • Assessment of their impact on TPV reliability • Refinement of models and their experimental validation	• Validation of TSV reliability models • Characterization of defects in bulk glass samples • Stress characterization with Raman spectroscopy	• Accuracy of material models • Discrepancy in geometries between models and experimental samples • Statistical variation in defect size and the corresponding reliability • Detecting submicron defects and their growth inside TPVs • Glass is not Raman active	Reliability characterization, failure analysis • Electrical characterization in both DC and RF domains • SEM Characterization of TPV defects, glass cracking and delamination • Direct stress measurements with Raman spectroscopy Validation of models

A schematic cross-section of TPV with combinations of various materials, geometry and process parameters that are studied is illustrated in Figure 1.12.

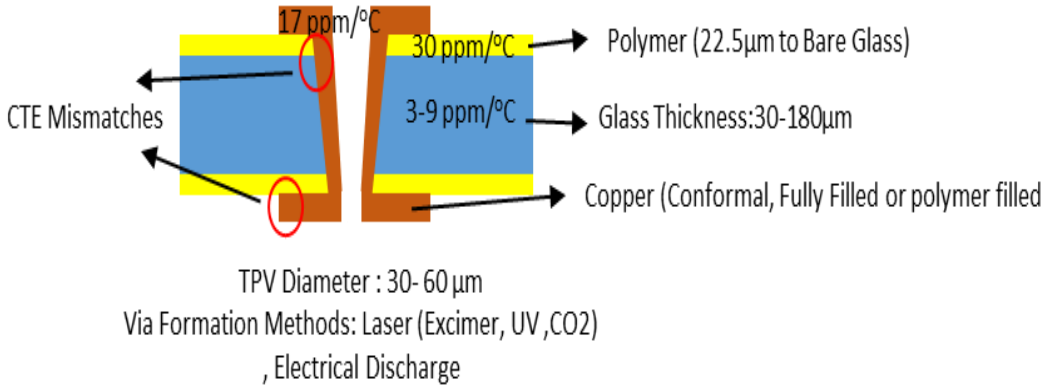


Figure 1.12. Schematic cross-section of TPVs

The research details are organized into the following chapters. Following the introduction and objectives in chapter 1, chapter 2 summarizes the relevant research on vertical interconnections, through-via formation options in glass and reliability characterization of copper TPVs in glass packages. Chapter 3 describes the mechanical modeling and design of TPVs in glass. In Chapter 4, design, materials and fabrication processes to form test vehicles are described. Reliability characterization and failure analysis of TPVs after accelerated testing are discussed in Chapter 5, along with direct stress measurements in glass by Raman spectroscopy to validate mechanical models. The last chapter summarizes the key contributions and suggestions for future work.

CHAPTER 2

LITERATURE SURVEY

The previous chapter discussed the motivation for a study in reliability of TPVs in glass interposers, and defined the research objectives, fundamental challenges and research tasks. This chapter summarizes the prior art literature on interposer technology and reliability of through-vias in interposers.

An interposer is an electronic substrate that provides ultra-high density interconnections between ICs either in 2D or in 3D format as illustrated in Figure 2.1. Interposers act as a space-transformer to spread a connection to a wider pitch to bridge the interconnection gap between ICs (<40 μm I/O pitch) and organic packages (~120 μm pitch) [19]. As introduced in Chapter 1, the escalating costs, thermal and performance challenges with advanced semiconductor nodes has steered the semiconductor industry to interposers for high-performance applications such as networks, servers, CPU, GPU and servers, and also mind-range products such as basebands, processors. In order to address this increasing demand for higher bandwidth at smaller form factor, interposers should be capable of facilitating high-density horizontal interconnections called redistribution layers (RDL) and vertical interconnections called through-package-vias (TPVs).

TPVs enable ultra-short interconnection length and ultra-high interconnection density between logic and memory ICs just like in 3D IC stacks with through-silicon-vias (TSVs), but at a lower cost. However, interposer materials should have ideal electrical, thermal and mechanical properties, in addition to low cost manufacturing processes for TPVs and RDL. Among various material candidates, organic materials, silicon and glass appear to be possible choices for developing high–density interposers. Interposers made out of these materials have specific

benefits and disadvantages. Fine-pitch through-package-via technology is the key element in realizing high-density organic, silicon or glass interposers. Furthermore, need for higher density vertical I/O imposes a trend for reducing TPV diameter and pitch that gives rise to reliability concerns. Therefore, there is compelling need to study reliability of TPVs through modeling and experiments, and thus to develop geometry, material and processing guidelines to achieve reliable TPV structures in organic, silicon and glass interposers.

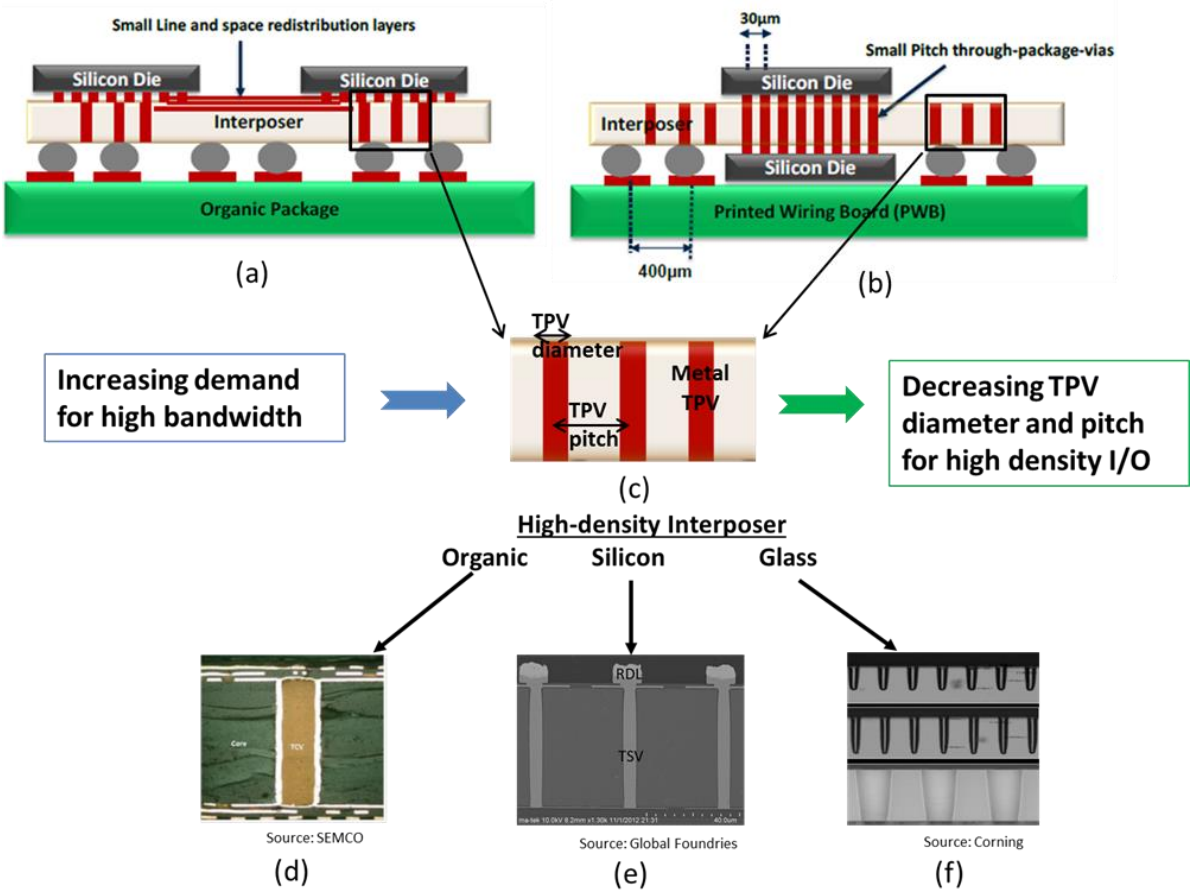
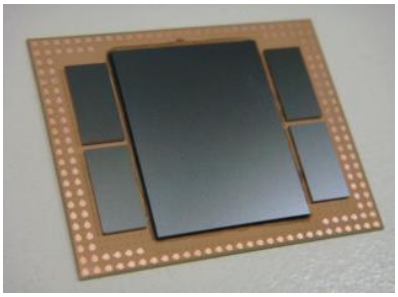


Figure 2.1. Cross-section schematic of a) 2.5D interposer with side-by-side integration, b) 3D interposer with double-side integration, c) Through-package-vias (TPVs) in d) organic interposer, e) silicon interposer and f) glass interposer

Modeling, design, fabrication and reliability of vertical interconnections in organic and silicon interposers have been extensively investigated. However, limited numbers of studies on reliability of TPVs in glass interposers have been reported. The following section reviews these advances.

2.1. Organic Interposers

Organic laminates are commonly preferred as interposer substrate materials because of their low cost, and existing manufacturing infrastructure and supply chain. Large panel processing on organic cores enables larger number of unit interposers per panel, thus reducing cost. Existing silicon fabrication and panel manufacturing processes can be leveraged for production of high-density organic interposers. However, organic interposers face two fundamental challenges in achieving finer I/O pitch: layer-to-layer mis-registration during copper RDL fabrication due to the poor thermo-mechanical stability issue of organic laminate cores, and warpage during chip assembly on thin core substrates due to low modulus of organic materials. This dimensional instability prohibits them from supporting high density I/Os with fine pitch interconnections and requires large capture pads for through-package-vias and microvias in organic interposers [20]. In order to address these challenges, organic laminates with high glass transition temperature (T_g), low CTE and high elastic modulus are currently being developed. Furthermore, residual stresses on organic laminate core during build-up processes are reduced by using thin film dielectrics and copper RDL. Kyocera demonstrated advanced organic interposer technology for 2.5D interposers to address the increasing need for high density I/O as shown in Figure 2.2.



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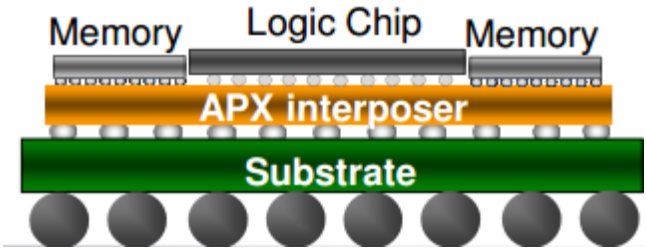

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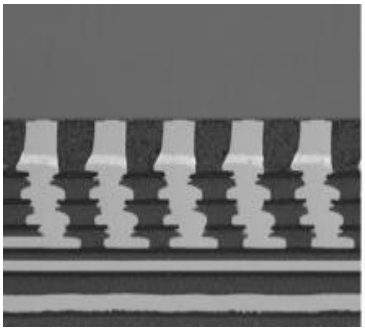

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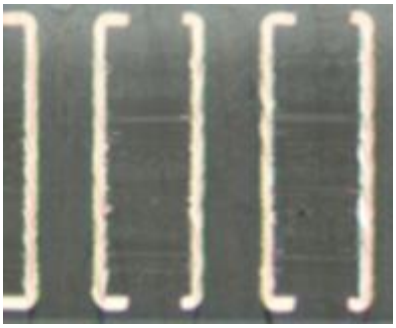

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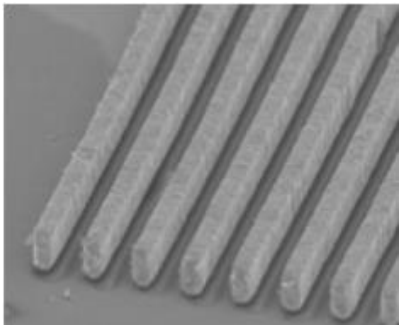


(e)

Figure 2.2. (a) Kyocera APX 2.5D organic interposer , (b) Cross-section schematic and enabling technologies that are (c)microvias (d) through-vias (e) fine-line RDL [21]

With development of low CTE, high modulus and low loss tangent organic materials, organic interposers offer a compelling lower cost alternative to silicon interposers for high performance applications. One of the key enabling blocks of high-density organic interposers is the plated through-hole in the organic laminate core. Trend in plated through-hole sizing is shown in Figure 2.3. There is continual push towards smaller diameters and smaller pitch that challenges the capability of organic substrates due to their limited thermal stability. Vias in low-CTE organic laminates experience high CTE mismatch that are more prone to failure compared to vias in silicon or glass.

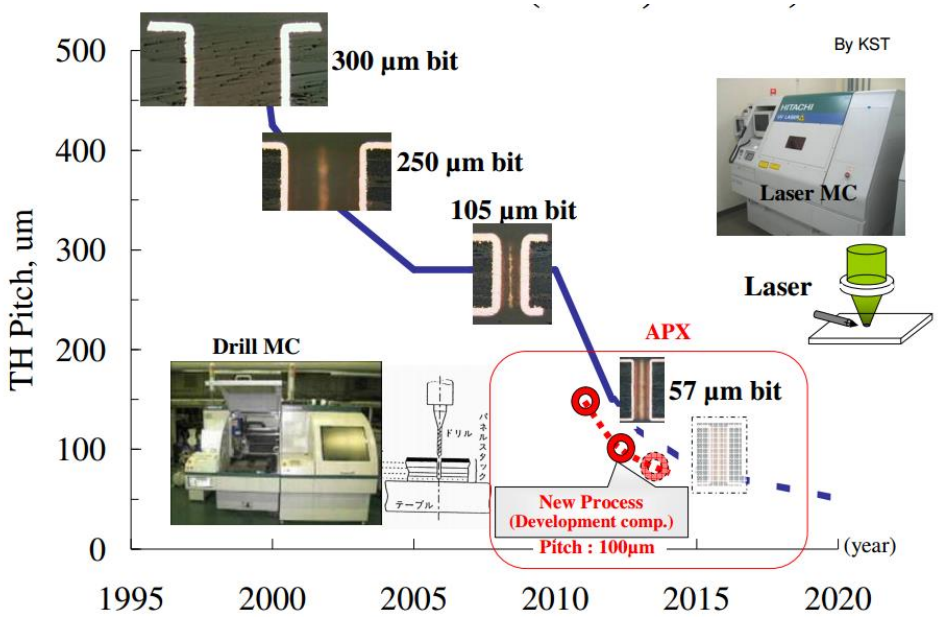
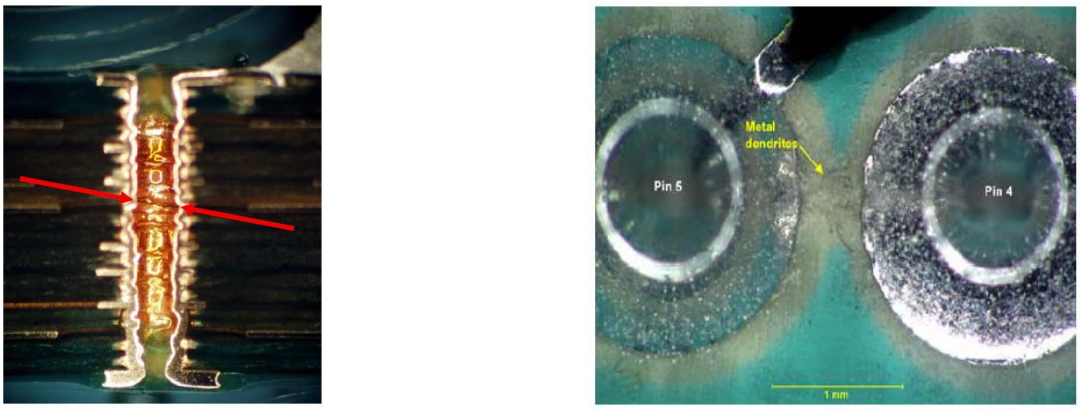


Figure 2.3. Pitch trend in plated through-holes in organic interposers [22]

2.1.1. Reliability of Through-Vias in Organic Interposers

As plated through-holes in organic substrates and microvias in dielectrics exist since 90s, there is extensive literature on modeling and reliability of these vertical interconnect structures. Hillman studied reliability of plated through-holes in organic laminate cores by finite element modeling, leading to design guidelines, fabrication of samples and accelerated life testing [23]. His modeling studies showed that the maximum strain in copper occurs in center of the PTH under extreme thermal cycling conditions. Due to the high CTE mismatch between organic core and copper, fatigue failures of copper were observed, as shown in Figure 2.4. As a result, plating quality needs to be carefully controlled for achieving high via-reliability. Thickness of plated copper and its elongation properties were also determine the via reliability. Moreover, plating process defects, such as voids and nodules, were shown to create stress concentrations leading to micro cracks in copper. Furthermore, moisture-induced chemical degradation was observed between adjacent plated through-holes with opposite electrical bias.



(a) **(b)**

Figure 2.4. (a) Circumferential cracking in copper, (b) electrochemical migration failure due to surface degradation [24]

Goyal investigated the reliability performance of conformal plated through-holes when subjected to thermal cycling tests [25]. Electrical opens were observed during initial 1000 thermal cycles between -55^{o}C – 125^{o}C and -65^{o}C-150^{o}C. Failure analysis revealed barrel cracking around the center of PTH as the main cause for electrical failures, as shown in Figure 2.5. Filling the PTH with solder was proposed to mitigate the cracking of copper.

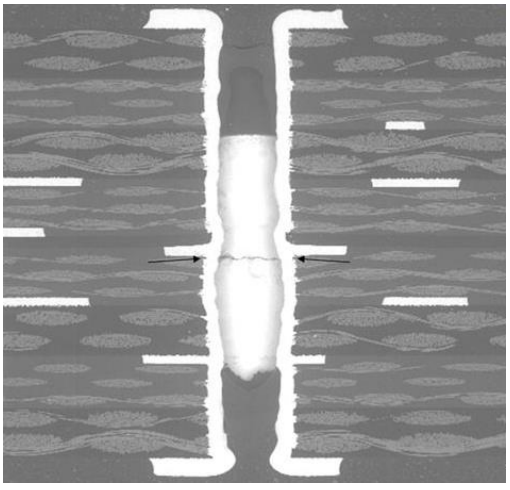
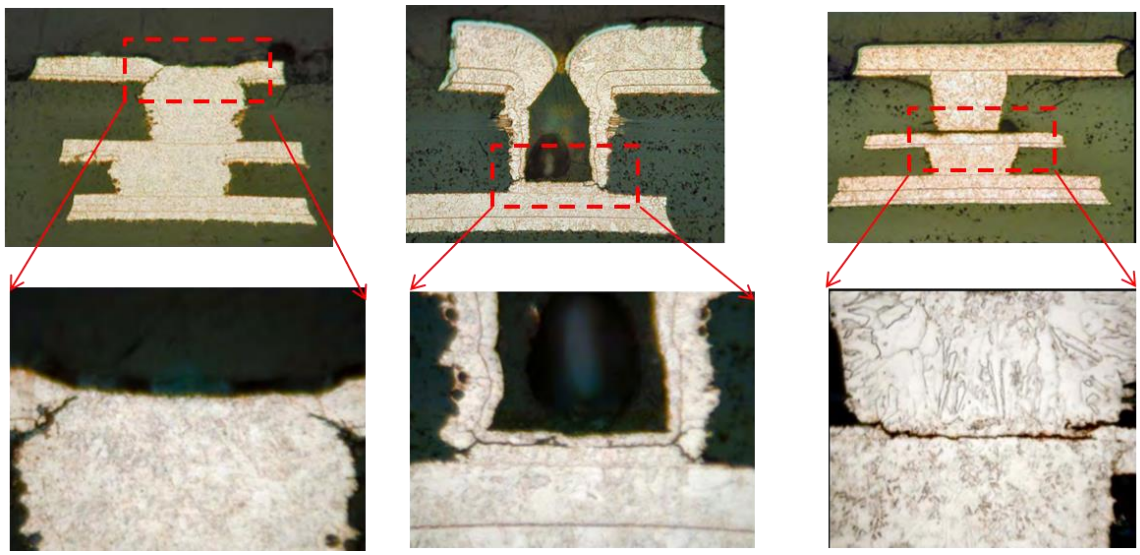


Figure 2.5. Circumferential barrel crack formation in a plated though hole [26]

Ramakrishna studied reliability of microvia structures fabricated in multilayer organic substrates through FEM modeling and reliability tests [27]. Effect of geometric features and materials on reliability of microvias was investigated. Both 2-D and 3-D models were built. It was pointed out that, for sufficiently large distances between microvias, 2-D models accurately describe the distribution of thermal stresses with lower computational cost compared to 3-D models. For fatigue life of microvias, a strain range-based approach was developed to predict the lifetime of tested microvia structures. Microvia failures were observed in microvia pad corners and in base of microvia where high stresses were predicted from modeling as shown in Figure 2.6 [28]. Also, interfacial separations between the base of the microvia and the target pad were commonly observed in stacked microvia structures that were attributed to quality of electroless plating on target pad before metallization of subsequent layer.

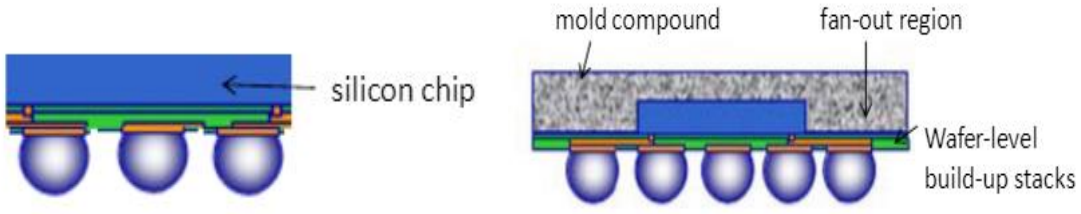


(a) **(b)** **(c)**

Figure 2.6. Failure modes in microvias (a) target pad cracks due to expansion (b) base cracks due to thin copper and (c) interface separation due to electroless plating issues [28]

2.1.2. Fan-Out Packaging

Fan-out packaging technology is one of the latest innovations to address the interconnection gap between printed circuit boards (PCBs) and ICs as die shrinkage reduces the ball grid array (BGA) pitch to accommodate high density I/O. Unlike fan-in, fan-out allows for the redistribution of the I/Os beyond the chip footprint. A traditional fan-in wafer-level package and a fan-out wafer-level package are shown in Figure 2.7.



(a) **(b)**

Figure 2.7. (a) Fan-in WLP and (b) fan-out WLP [29]

With fan-out technology, a higher integration level and a greater number of external contacts are provided for semiconductor devices at a smaller form factor along with improved thermal and electrical performance [30]. Therefore, as an alternative solution to organic interposers, it eliminates the need for a substrate and also lead to substantial cost reduction, as illustrated in Figure 2.8. With fan-out approach, through-package-vias in organic laminate core are also eliminated, thus cost and reliability issues associated with through-vias are avoided.

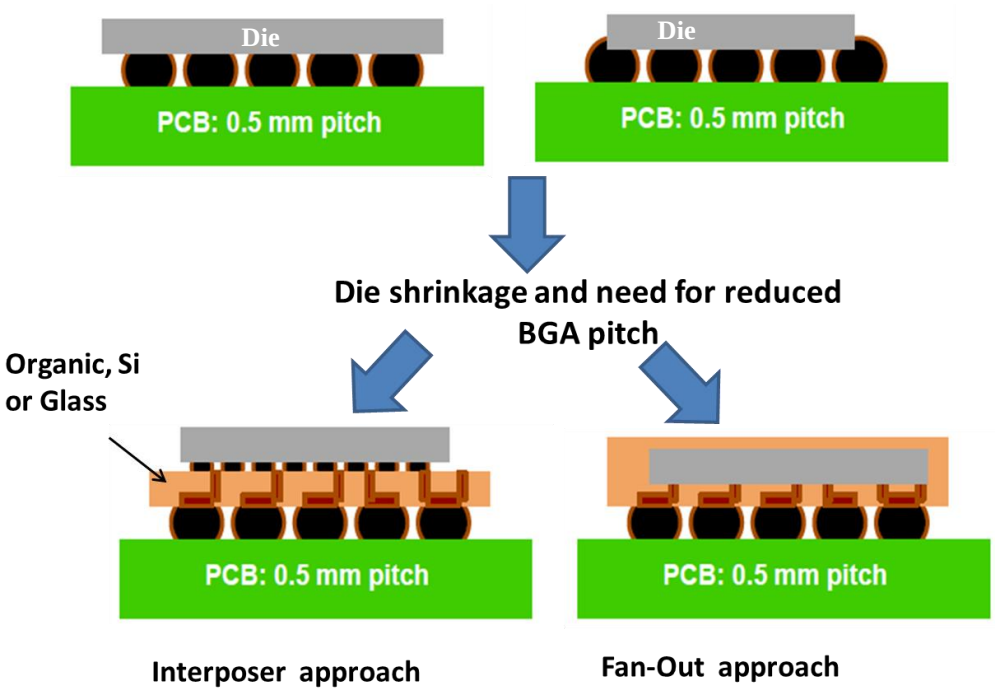


Figure 2.8. Fan-out technology as an alternative to interposer based approach when PCB cannot support the shrinkage in dimensions of IC dies [31].

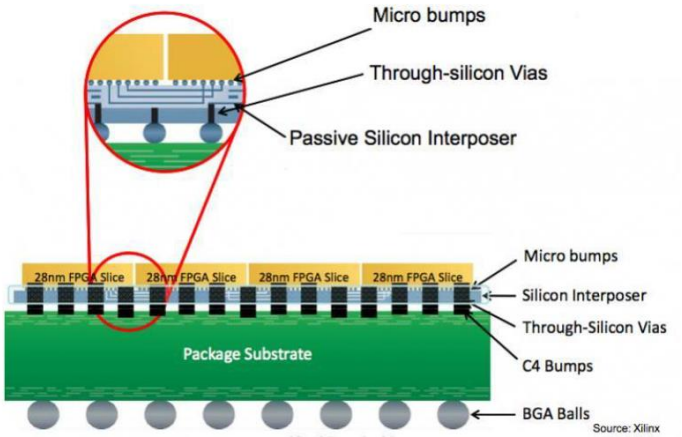
Fan-out packaging is performed either at wafer-level or panel-level. In Fan-Out wafer-level packaging (FOWLP), individual dies are embedded in a low-cost material such as epoxy mold compound (EMC) with space allocated between each die for additional I/O connection points, thus avoiding the use of relatively expensive Si real estate to accommodate a high I/O count. Redistribution Layers (RDL) are formed using PVD seed deposition and subsequent electroplating/patterning to re-route I/O connections on the die to the mold compound regions in the periphery. Therefore, a surface mount device (SMD) compatible package is obtained from a reconfigured molded wafer combined with thin film redistribution layers.

Main advantages of FOWLP are its thinness from its substrate-less package, low thermal resistance, improved RF performance due to shorter interconnections, together with direct IC connection by thin film metallization instead of wire bonds or flip chip bumps and lower parasitic effects [32]. In addition, the redistribution layer can also provide embedded passives and antenna structures using a multi-layer structure for heterogeneous integration. The drive for cost reduction with enhanced performance is also shifting the electronics industry from wafer-scale processing to panel-scale format. To further bring down the unit package cost, fan-out panel level packaging (FOPLP) is developed to utilize 18”x24” panels instead of 300 mm wafers, thus leading to higher throughput and production volume. This manufacturing can reduce cost by leveraging tools from wafer fabrication as well as those from PCB, flat-panel display and photovoltaic industries. Despite these advantages of fan-out packaging, manufacturing and reliability challenges related to use of epoxy polymers in mold compound and subsequent stack-up layers still impose limitations. Polymer materials with adjusted CTE, modulus, low shrinkage, low moisture absorption and outgassing are required to mitigate potential warpage issues during wafer reconstitution.

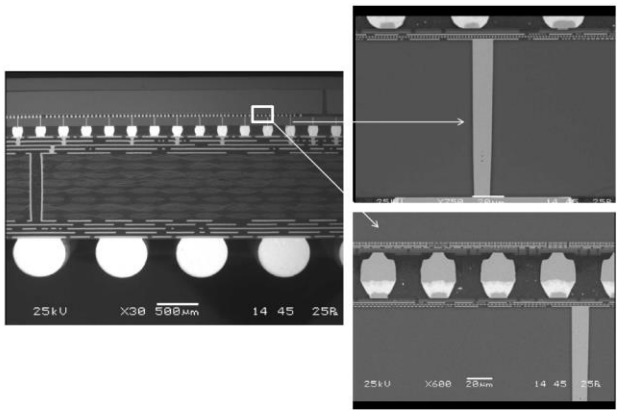
2.2. Silicon Interposers

To address these shortcomings of organic laminates and fan-out packages related to their dimensional stability issues, silicon interposers are explored with standard back-end-of-line (BEOL) wafer processes to achieve the required wiring and I/O density. The early silicon interposers, developed by IBM and Bell Labs in 80s, were fabricated on smaller wafers with copper-polymer re-distribution layers, but without TSVs, and had to be interconnected to the system using wire bonds [33]. The development of TSV processes in 90s led to thin silicon interposers with TSV interconnections to organic packages and printed wiring boards. High

thermal stability and surface smoothness of silicon interposers facilitate high I/O density through fine-line RDL and fine-pitch through-silicon-vias (TSVs). A recently-developed silicon interposer with TSVs from Xilinx is shown in Figure 2.9, along with BGA and TSVs enabling the wide I/O interface.



(a)



(b)

Figure 2.9. (a) Schematic drawing of silicon interposer from Xilinx, (b) SEM image of BGA and TSVs [34].

Although silicon interposers overcame the challenges of organic packages, they pose a different set of challenges such as high cost due to limited wafer size (200-300mm). Limited

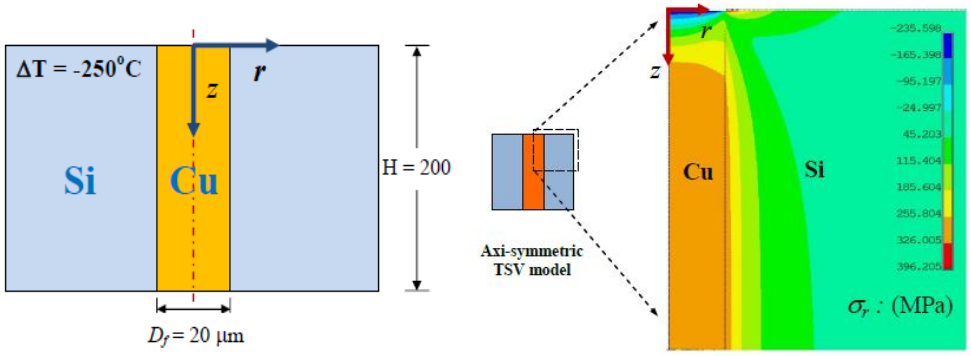
wafer size yields fewer large interposers per wafer. In addition, the cost of insulating liners for electrical isolation of via conductors is quite high. The high cost is attributed to single-side processes as well as the need for back-grinding and polishing to achieve thin Si interposers. Back-End-of-Line (BEOL) process technologies such as physical vapor deposition (PVD), chemical vapor deposition (CVD) and Bosch reactive ion etching (RIE) for TSVs are typically used, which also lead to higher cost.

2.2.1. Reliability of Through-Vias in Silicon Interposers

A fundamental challenge for silicon interposers with TSVs is the thermomechanical reliability, driven by the difference in CTE mismatch between copper and silicon. TSV insulating liner, such as thermally grown and brittle SiO_2, is subjected to high thermomechanical stress, leading to reliability concerns. Many studies reported mechanical modeling and reliability analysis of TSVs in silicon [35-38].

Distribution of thermal mismatch stress around a metal in a brittle matrix can be considered as a superposition of two classical mechanics problems with known solutions [39]: 1) Lame's stress distribution with 2-D plane strain assumption [40], 2) Boussinesq stress distribution due to surface pressure [41]. Ryu applied this superposition concept to TSVs in wafers and semi-analytically calculated the 3-D near-surface stress distribution in TSV by adding up the solutions to each problem [42]. Plane-strain 2-D solution can only predict stresses far away from the wafer surface, while the semi-analytical 3-D solution is a good approximation everywhere for vias in thick wafers with aspect ratio higher than 10, not applicable to thin wafers. FEM models of TSV were developed to compare the stress distribution, as shown in Figure 2.10. It is seen that the maximum radial stress occurs on the wafer surface at a short distance away from the edge of TSVs, a characteristic that is also observed in the FEA

simulation. In contrast, at a depth of $z=D_f/2$, the maximum radial stress occurs right at the edge of TSV. At this depth and at surface, 3D semi-analytic solution matches the FEA. At deeper than 5Df away from the top surface, the stress state approaches the 2-D Lame distribution based on plane-strain equation.



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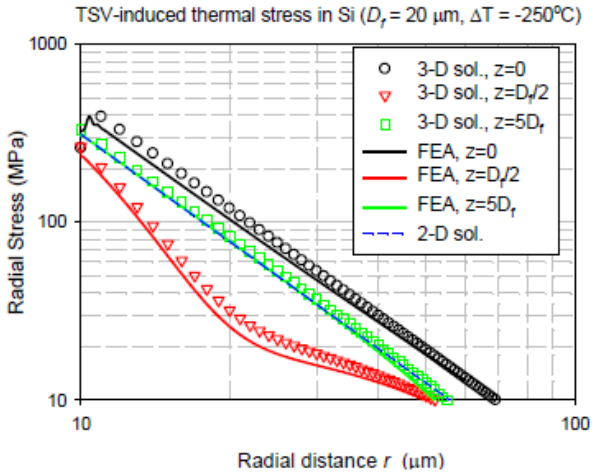
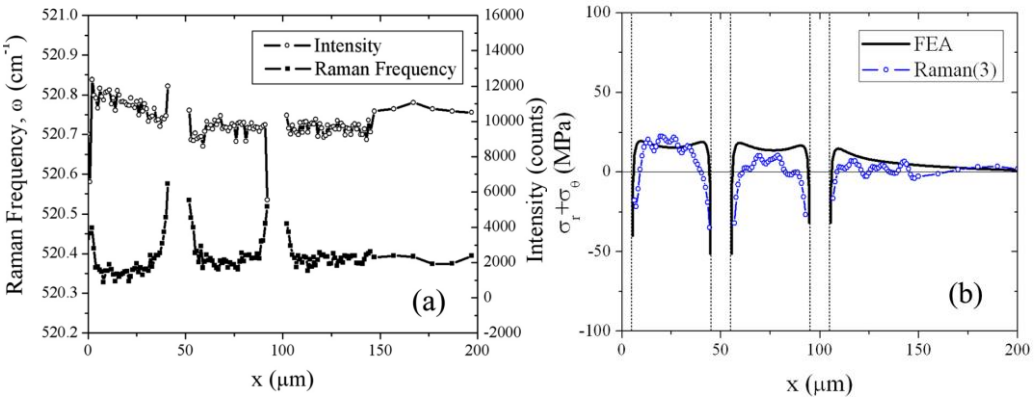


(c)

Figure 2.10. (a) Illustration of the cross-section of an axi-symmetric FEA model for thermomechanical simulation, (b) FEA simulation of the radial stress, (c) comparison between semi-analytic stress solution and FEA simulation [43]

As silicon is a Raman-active material with distinct stress-sensitive peak around 521 cm^{-1}, Micro Raman spectroscopy is used to measure near-surface stresses around TSVs. Using the equation relating the peak shift to stress components, stresses were estimated. Results from FEM analysis were matched to stresses calculated on Raman peak shift measurements on the silicon surface in vicinity of TSVs as shown in Figure 2.11.



(a) (b)

Figure 2.11. (a) Measured Raman intensity and peak frequency for 2 TSVs with shifts at the TSV edges shown with dashed lines, (b) Comparison of the near-surface stress distribution between Raman measurements and finite element analysis [44]

Lu used the aforementioned semi-analytical equations for 3-D stress distribution in TSVs in order to analytically calculate energy release rates for delamination of copper from silicon both on the surface and also along the via sidewall [45]. It was reported that using annular vias instead of fully-filled vias reduce the radial peeling stress by a factor of $(1- n^2)$ where n is the ratio of inner diameter to outer diameter of the annular via. Therefore, energy release rate available for delamination of copper along the TSV sidewall also decreases, as shown in Figure 2.12. As seen, the energy release rate estimations based on analytical model and simulation

approach predict that the stresses reduce away from wafer surface. Also, with thinner plating leading to high inner diameter, it is possible to reduce the energy release rate up to a point where delamination of copper along TSV sidewall cannot occur theoretically. It was also pointed out that using a dielectric polymer, such as BCB instead of traditional SiO_2, facilitates improved adhesion of copper to TSV sidewall and also decreases the energy release rate for interfacial crack growth.

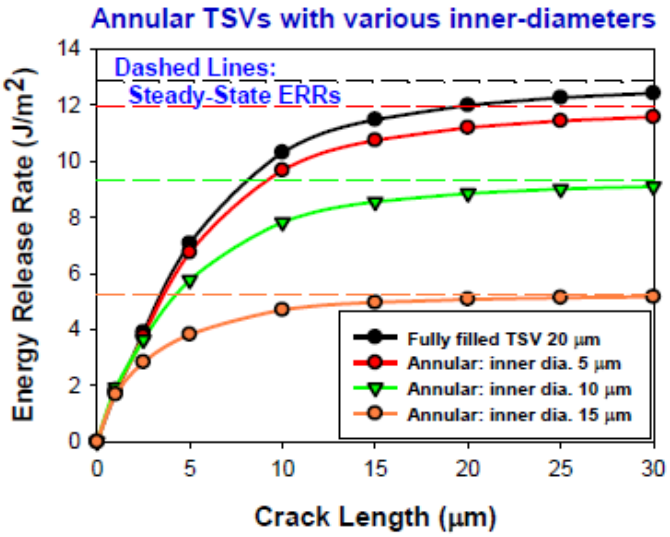
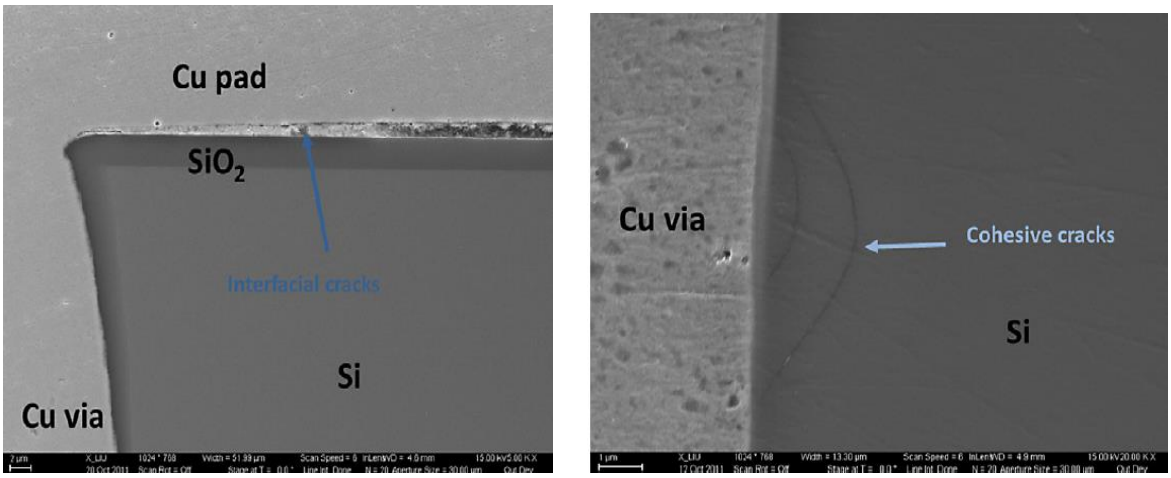


Fig.2.12. Energy release rates for delamination of copper from TSV sidewall with fixed diameter and changing plating thickness inside TSVs [46].

Liu have reported extensively on finite element modeling (FM) simulations of the thermal stress distribution in Cu-filled TSVs [47]. These models showed that the thermal stresses in SiO2 dielectric liner and the Cu/SiO2 interface, lead to failure mechanisms in TSVs, such as dielectric liner delamination and silicon cracking as illustrated in Figure 2.13.



(a) **(b)**

Figure 2.13. (a) Interfacial crack around SiO2 and (b) cohesive cracks in silicon [48]

TSVs with 40 µm diameter and 260 µm height were fabricated and characterized to verify modeling results. X-ray diffraction (XRD) was used to measure the average stress in silicon and to determine the stress-free temperature of Cu. These parameters were plugged in to FEM models to improve accuracy. The TSV samples that were thermal-shocked for 4000 cycles showed both delamination on Cu/SiO_2 interface and crack in SiO_2. Cohesive cracks were observed to initiate from brittle SiO_2. They grow in a semi-loop pattern and return back to the high stress Cu/SiO_2 [49]. This behavior was explained by finite-element crack growth simulations, showing that crack follows the path in that the stress intensity factor is higher. Therefore, the cracks cannot grow radially and reach the adjacent TSV due to decreasing stress intensity factor along the radial direction.

Replacing brittle SiO2 with a low-modulus SU-8 polymer helped to improve TSV reliability due to a "cushion effect" as shown in Fig. 2.14. This aforementioned cushion effect was also demonstrated by Chen using TSVs in polycrystalline silicon interposers [50]. TPVs were first drilled on bare polycrystalline panel, and then laminated with polymer on both sides.

Polymer filled these via holes, which are then again drilled by a second laser ablation step. This process resulted in TPVs with polymer liners along the sidewalls, which significantly reduced the stress on silicon. Therefore, SiO_2 and Si cracking failure, which was previously observed with traditional TSVs, were prevented.

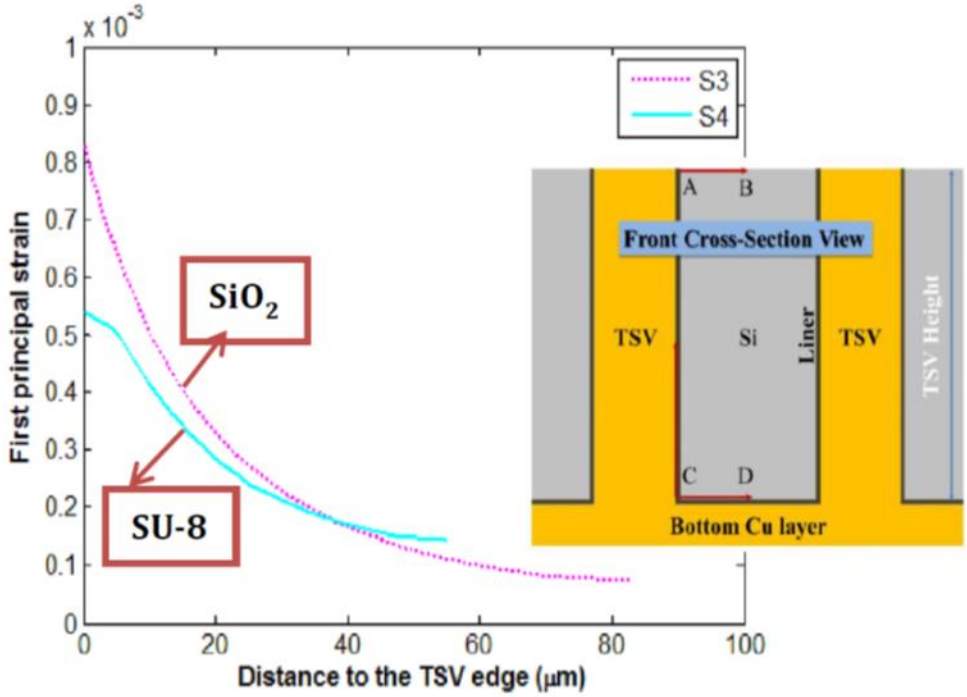
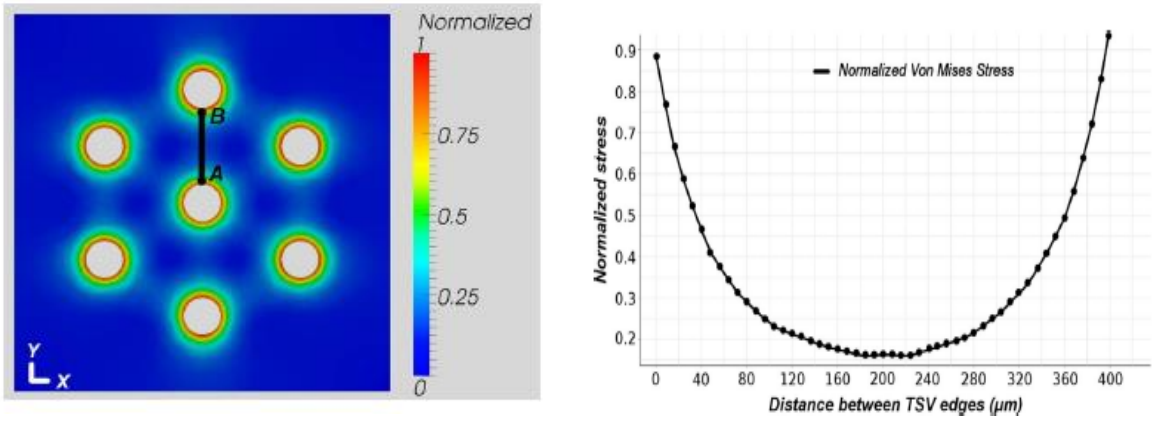


Figure 2.14. Cushion effect due to polymer liner (first principal strain in copper) [51]

Cassidy studied TSV reliability with blind vias of 250 µm depth and 100 µm diameter at 400 µm pitch [52]. The oxide liner has a thickness of 400nm, and the conformal plated metal had a nominal thickness of 20 µm. Key parameters for reliability assessment, such as thermomechanical stress, leakage current and dielectric breakdown, were discussed. It was reported that the stresses localize around TSV side walls and tapers off in bulk silicon between TSVs as shown in Figure 2.15. In addition, the thin oxide liner was shown to be susceptible to problems such as current leakage due to cracking and breakdown due to high electric fields

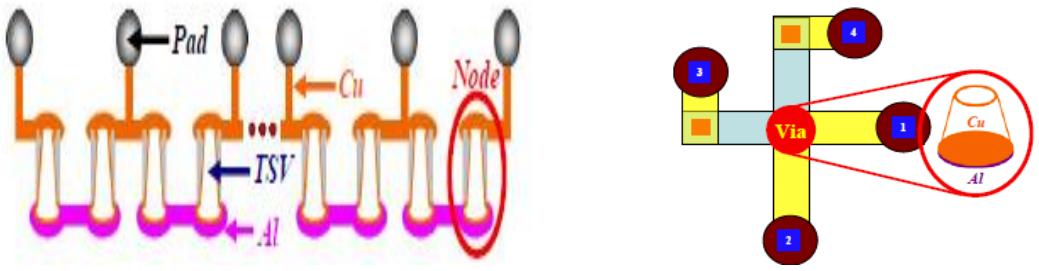
within. Sidewall defect density of TSVs was pointed to be a critical parameter for reliability while the possibility of failures directly depends on sidewall defects.



(a) **(b)**

Figure 2.15. Normalized Von Mises Stress Distribution for a group of seven TSVs, (b) Variation of von Mises stress from a TSV edge to the adjacent TSV [52].

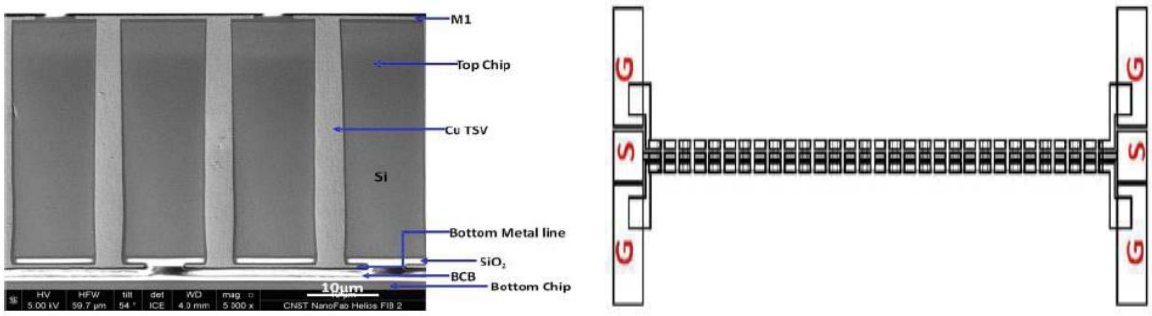
Chung explored the reliability of TSVs used for wafer level packaging of CMOS image sensors [53]. Several test patterns were designed for monitoring TSV chain resistance and leakage, as shown in Figure 2.16. Test samples were used to characterize the electrical performance of TSVs and the yield of fabrication process. Fabricated TSV diameters were 60 μm and 55μm and their resistances were measured as 7mΩ and 9 mΩ respectively.



(a) **(b)**

Figure 2.16. (a) TSV daisy chain structure and (b) Kelvin test structure for single TSV [53]

Chukwodi studied the reliability of TSVs using co-planar waveguides excited at RF frequencies, as shown in Figure 2.17. Waveguides consisted of 60 TSV transitions.

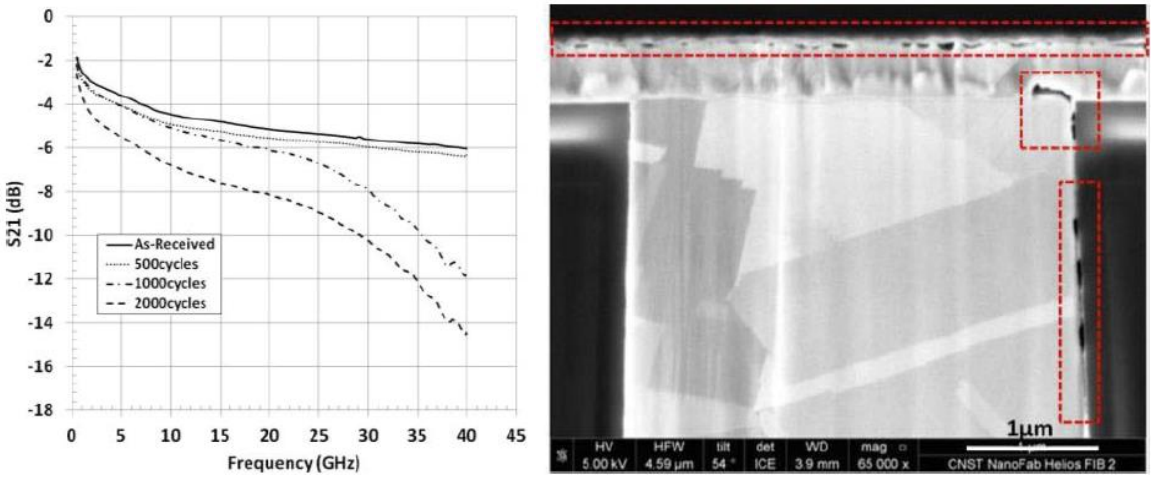


(a) **(b)**

Figure 2.17. (a) TSV daisy chain structure, (b) forming the CPW line in GSG configuration [54]

Scattering parameters of the transmission line was measured at certain intervals. A decrease in S_{21} was observed especially for frequencies higher than 20 GHz after 1000 thermal cycles. This increase was linked to the formation of voids along the copper and TSV dielectric interface as shown in Figure 2.18, causing scattering of RF signals. DC-based method is only

sensitive to failures in conducting pad, whereas RF methods are sensitive to distortions in conductors, dielectrics and semiconductors.



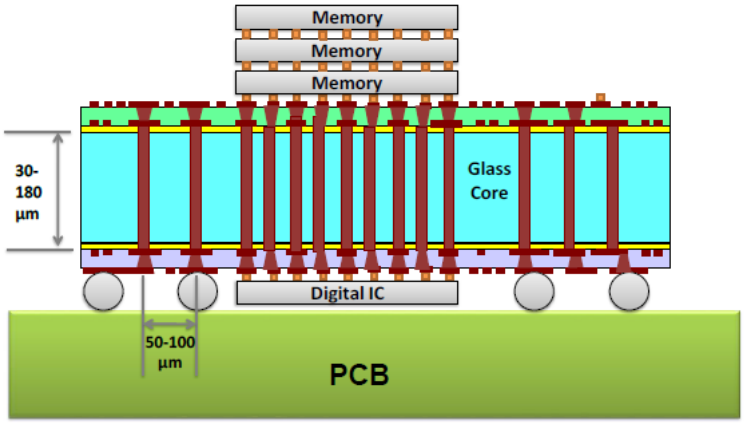
(a) **(b)**

Figure 2.18. (a) Deterioration in S_{21} of the CPW after thermal cycling test due to (b) void formation along the Cu/dielectric interface as seen in FIB cross-section [55]

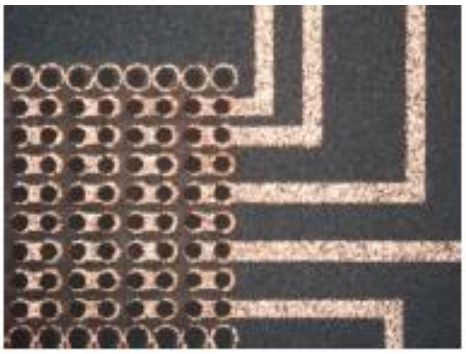
2.3. Glass Interposers

Although, silicon interposers can address certain performance challenges to some extent, they still suffer from poor electrical performance because of the semiconducting nature of silicon and high cost associated with TPV formation, wafer-scale Back end of line (BEOL) processes and the need for thick insulation linings on silicon [56]. To address the above challenges associated with silicon interposers, glass appears to be an ideal interposer material. High dimensional stability and smooth surface of glass facilitate high I/O density. High electrical resistivity of glass eliminates the requirement for insulating liners in via wall and leads to high electrical performance. Furthermore, availability of glass in large panel format offers potentially

low manufacturing cost. Glass offers very low thickness for reduced form-factor, ability to define small features for high-density integration, mechanical stability for multi-component assembly, approximate CTE match to silicon die and printed circuit board (PCB) materials for reduced thermo-mechanical stresses, and large-panel processability for low cost [57]. A glass interposer is shown in Figure 2.19 along with basic building blocks.



(a)



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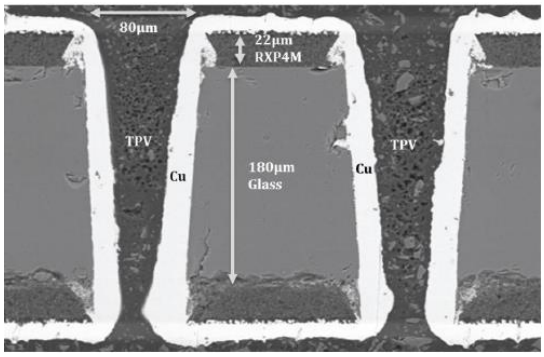
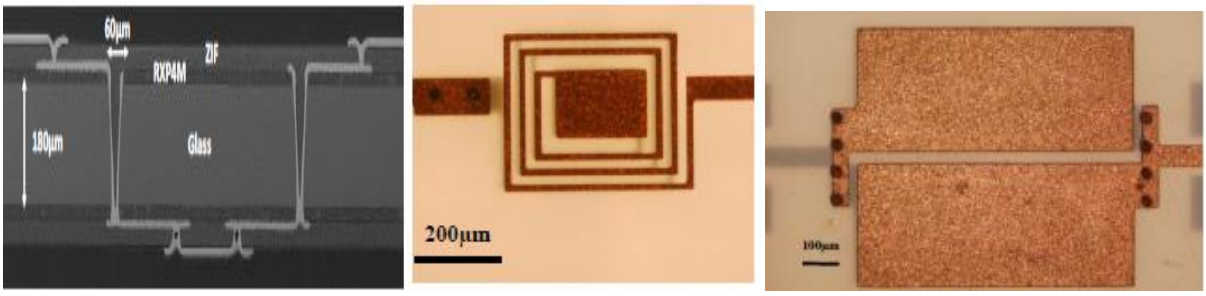


(c)

Figure 2.19. (a) Cross-section schematic of glass interposer along with basic building blocks (c) fine-pitch RDL as horizontal interconnections and (d) TPVs as vertical interconnections [58]

Previous studies focused on utilizing electrical properties of glass in order to demonstrate RF modules with superior performances and transmission lines with lowest loss. Glass is an ideal

material for RF applications due to its excellent dimensional stability, surface flatness, and low-loss. In addition, it is possible to design passive devices with high 'Q' factors on glass substrates. Sitaraman et.al, demonstrated high quality low pass RF filter consisting of spiral inductors and parallel plate stitched capacitors connected by through-package vias on a four-metal layer glass interposer as illustrated in Figure 2.20.



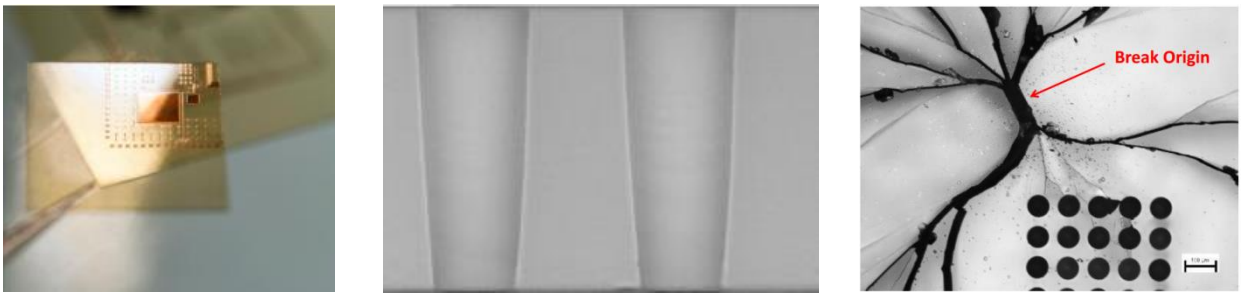
(a) **(b)** **(c)**

Figure 2.20. (a) Cross-section of 4 metal layer glass interposer (b) spiral inductors (c) parallel-plate stitched capacitors on glass [59]

Fraunhofer IZM explored glass-based electronic and photonic modules with through-glass-vias (TGVs) fabricated using femto-second and excimer laser ablation [60]. The glass substrates used for the TGV study had a thickness value of 400µm or 500µm to facilitate handling during processing. The Ti: sapphire femtosecond (fs) laser helped achieve through-holes with an entrance diameter of 99µm in 500µm thick glass. On the other hand, TGV formation using excimer lasers with nano-second pulse duration yielded smaller via diameter at the entrance (48µm) compared to fs lasers. This implies that the highest aspect ratio of TGVs achieved using the above ablation techniques was approximately 5:1. Sputtered and electroless copper deposition were used to form the conductive seed layer for direct metallization on the

glass surfaces. In addition to the electrical interconnections, optical waveguides were fabricated on the glass surface through an ion-exchange process using silver ions. The silver ions replaced the sodium within the glass matrix and provided a graded refractive index necessary for optical wave confinement. The work on such photonic modules has focused on thicker glass substrates (400-500μm) that are significantly easier to process compared to the ultra-thin glass substrates (30-100μm) proposed in this research.

ITRI in collaboration with Corning have investigated the fabrication of glass interposers using wafer-based processing methods that are commonly used for silicon interposer fabrication [61]. Through-vias with a diameter of 30μm were formed in 100 μm thin glass substrates by Corning. Subsequent metallization of the TPVs was achieved using a combination of sputtered seeding (Ti/Cu) and copper electroplating. Wafer thinning was performed on the glass substrates to reveal the TPVs on the backside and RDLs were lithographically patterned after flipping the glass wafer. PBO was used as the passivation layer between RDL layers on each side of the interposer. The line width on the RDL layers was limited to a minimum value of 20μm in the above study. Strength of glass with through-vias was characterized using ring-on-ring test. During the strength test, glass breakage did not originate from through-via array, which demonstrates the quality of the via formation method as shown in Figure 2.21.



(a) **(b)** **(c)**

Fig.2.21. (a) Glass interposer by ITRI , (b) TPV formations, (c) glass breakage not originating from via during ring-on-ring test [62]

Keech et.al, demonstrated via-first formation and metallization process of blind vias with 25 µm diameter on 300 µm thick glass wafers [63]. Metallization was achieved by sputtering of adhesion layer and copper seed layer followed by electroplating. Glass wafers were then background to 100 µm. However, back grinding increases the fabrication time, cost, and may create defects that compromise mechanical integrity. This process is also not panel-scalable and leads to waste of material. Sputtering titanium followed by copper is well-known via-first seed-layer metallization process to form TPVs in glass. However, sputtering process limits the minimum diameter of TPV that can be metallized thoroughly. Ogutu et al demonstrated a method to address this issue with an additional subsequent electroless plating step after sputtering, to ensure metal deposition throughout TPV hole [64].

2.3.1. TPV Formation in Glass

Glass as an interposer technology has been explored recently owing to its favorable material properties. The fundamental barrier to ultra-thin glass interposers, which is the defect-free formation of small vias in close proximity to each other, has been largely overcome recently by Georgia Tech and its industry partners.

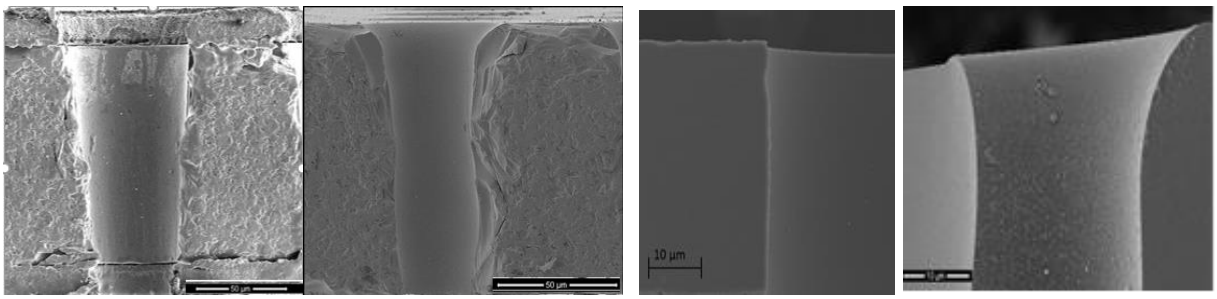
Sukumaran studied laser drilling as a method to form high-quality vias in glass at high throughput [65]. Feasibility of different lasers including UV, CO2 and ArF based excimer were explored. ArF based excimer lasers operating at 193nm were found to be comparatively more effective, inducing minimum thermal stress during the ablation process. No micro-cracks were observed on the glass surface or along the side wall after laser ablation. Since glass has high absorption at 193nm, almost 95% of the laser energy is utilized to break the chemical bonds

within the glass matrix. A small part of the laser fluence is converted into heat energy, which is negligible, and thus the thermal stresses are also minimal. This process was shown to form multiple vias at one time by using mask projection method. Drawback of this method was the slow speed of via formation requiring using ultra-thin glasses.

Researchers at Asahi Glass Company (AGC) studied focused electrical discharge to form vias in glass [66]. Focused and controlled electrical discharging was applied to glass to create locally molten region. Then, dielectric breakdown of glass was induced together with internal high pressure by heat to evaporate and eject molten glass. This method was shown to be capable of forming high aspect ratio TPVs at ultrafast speed. Drawback of this method was its inapplicability to polymer-laminated glass.

Chen studied excimer laser ablation on glass using mask projection. The glass surface morphology was studied as a function of repetition rate, and the results on glass were compared to those obtained on polyimide and silicon [67]. The work primarily focused on via formation in thicker glass substrates (500μm).

Corning has developed a method to form vias in glass at high throughput using laser assisted etching [68]. With this method vias with 30 μm diameter was demonstrated at 150 μm thick glass substrates. To improve the strength of glass wafers with vias, Corning has developed a method of introducing compressive stresses on the glass surface using an ion-exchange process. The fracture toughness of glass with vias was reported to have significantly after the exchange process. Glass substrates with vias were subjected to 3-point bending test and it was observed that fracture patterns did not pass through the vias that demonstrated the quality of via formation technique.



(a) **(b)** **(c)** **(d)**

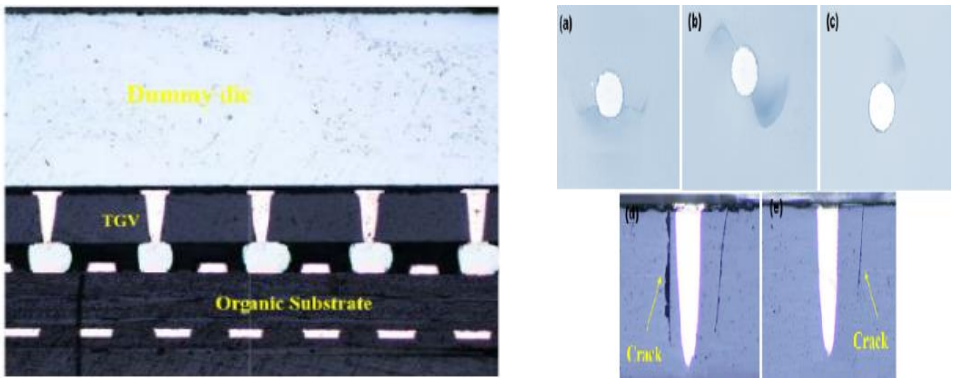
Figure 2.22. TPVs formed with different methods: a) Excimer Laser, b) CO_2 laser, c) Laser assisted chemical etching and c) Electrical discharge

In summary, there are various methods to form vias in glass. However, each technique results in a different via shape and defects as shown in Figure 2.22. Size and distribution of defects impact the reliability of vias. These via formation methods need to be qualified by reliability testing.

2.3.3. Reliability of Through-Package-Vias in Glass Interposers

Reliability of copper-plated vias in ultra-thin glass interposers is relatively new field; however, there are some related studies in literature. Wei investigated fabrication and reliability of a 3D stacking structure using through glass vias as major interconnect [69]. For via formation, laser drilling was used on 300µm thick glass and vias were metallized by Ti/Cu sputtering. Through glass vias were revealed by wet etching and thinning of the glass substrate down to 150 µm by chemical mechanical polishing. It was observed that chemical-mechanical polishing lead to warpage and crack formation in glass substrate as illustrated in Figure 2.23. Dummy test die was assembled on one side of the glass and this module was assembled to an organic substrate. A demonstration samples was subjected to 500 thermal cycles between -55^{o}C

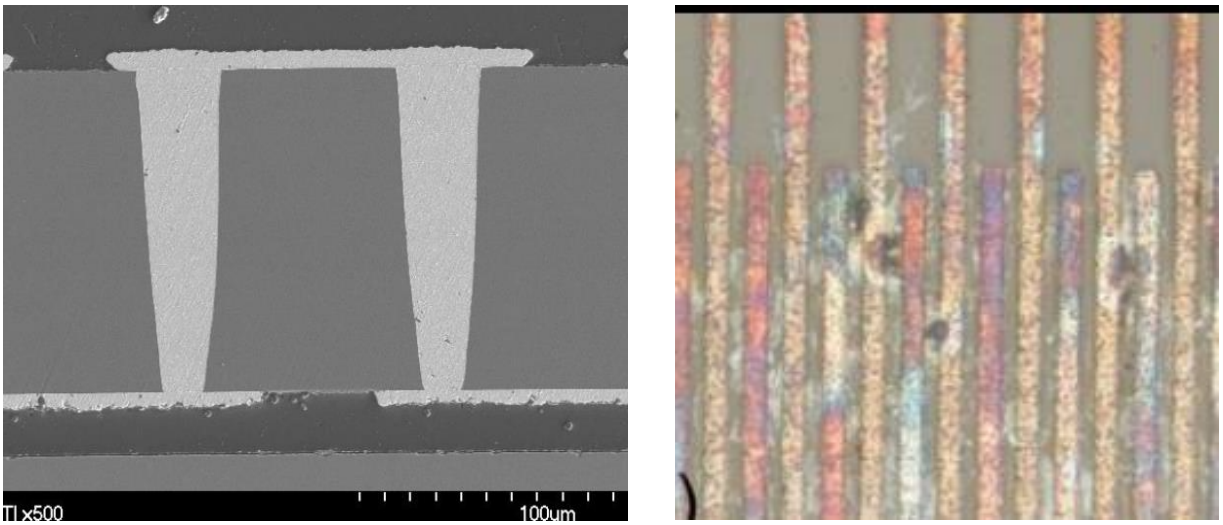
and 125°C and no electrical failures were observed ether in solder bumps or in through glass vias.



(a) **(b)**

Figure 2.23. (a) Cross-section of 3D glass interposer stack and (b) Cracks around TPVs due to CMP processes [69]

Lueck studied reliability of through-glass-vias in bare glass up to 1000 cycles from -40°C to 125°C [70]. Fabrication of glass interposer was achieved sing standard back end of the line (BEOL) tools. Metallization was achieved using metal-organic chemical vapor deposition (MOCVD) for seed-layer formation followed by electroplating. Via diameter was 35µm and glass thickness was 120µm. Through-glass-vias of 20x20 arrays were fabricated and metallized to form daisy chains. There were no electrical opens related to failures in copper and no cracks in glass were observed in physical analysis. However, biased-HAST test on interdigitated copper lines on glass surface revealed copper migration that resulted in degradation of insulation resistance. This result indicated that for glass substrates a barrier layer is necessary between the substrate and Cu metallization to prevent Cu migration.



(a) **(b)**

Figure 2.24.(a) Cross-section of TPVs after 1000 thermal cycles (b) copper migration on glass surface between biased fine line (70)

Benali analyzed reliability of copper plated-vias in glass using analytical equations and finite element modeling [71]. It was shown that diameter has a large effect on von Mises stress around via, and this stress value decreases with increasing diameter in conformal plated vias. It was observed that the glass thickness has relatively smaller impact on via stress compared to diameter and electroplated copper thickness. El Amrani investigated failure mechanisms of through-glass-vias under thermomechanical loading using Lock-in thermography for defect detection and localization [72]. Test samples were fabricated using double-side laser drilling with alignment problems that resulted in plating defects. These plating defects grew into larger cracks in copper that were observed as hot spots in thermographs as shown in Figure 2.25. When the plating defects were eliminated, no failures in copper were observed.

Most of the prior work on glass TPVs has focused on thicker glass substrates formed with laser-assisted chemical etching. A comprehensive study on reliability of TPVs in glass has not been studied yet in detail through modeling, design, fabrication and reliability characterization. This research aims to address this with a comprehensive study of TPV reliability in glass, starting from mechanical modeling and design, leading to experimental validation. This proposed research extends previous studies by studying reliability of TPV with 3 different aspects: 1) TPVs in polymer-laminated and bare glass formed with various via formations methods leading to different defect distribution and geometries 2) TPVs in free-standing glass interposers and with double-side assembly 3) Reliability characterization of TPVs in both DC and RF domain along with Micro Raman stress measurements.

CHAPTER 3

MECHANICAL MODELING OF TPVs

This chapter describes modeling of TPVs in glass to obtain design guidelines for achieving low TPV stresses compared to organic or silicon packages, and high fatigue life of over 3000 thermal cycles. Despite tailorability of glass CTE, the CTE mismatch between TPV materials such as copper, glass and polymer is unavoidable, as shown in Figure 3.1. This mismatch results in high stresses on glass walls as well as high strains in copper metallization during temperature excursions. Quantitative parametric analysis is essential to design the key material and geometric parameters for TPV reliability. In Section 1, analytical equations for thermomechanical stresses in TPVs are introduced, followed by their comparison with finite element modeling. Section 2 describes finite element models for TPV in polymer-laminated glass. The reliability of TPVs in bare glass are described in Section 3. Section 4 describes the via-first TPV with thin primer polymer. The impact of IC assembly on reliability of TPVs are documented in Section 5, while Section 6 covers TPVs with polymer-filling inside the hollow via and TPVs with polymer liners on the via wall. In Section 7, fracture models are used to predict crack growth during thermal cycling.

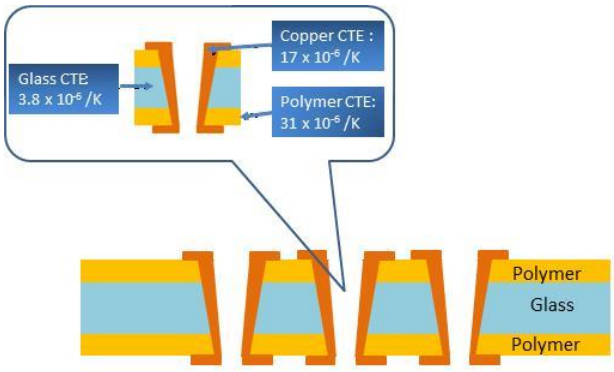


Figure 3.1. TPV creating CTE mismatch in glass interposer

Glass is inherently a very strong but brittle material. However, unavoidable defects that are formed during glass manufacturing, dicing and subsequent fabrication process steps significantly decrease the strength of bare glass. These inherent glass defects, especially on the bare glass surfaces, create stress concentrations leading to lower mechanical strength. The strength can be further reduced by defects related to TPV formation and metallization. As a result, brittleness of glass and the presence of copper-plated through-vias introduce reliability concerns that need to be addressed. This task focuses on analytical and finite element modeling of TPVs for lower stresses and high reliability in a variety of configurations: 1) TPV in polymer-laminated glass 2) TPV in bare glass 3) via-first TPV 4) TPV in 3D Package with double-side assembly. Parametric studies are performed to obtain the impact of various geometric and material properties on stresses around TPV and strains in copper. Thermomechanical models are developed to assess the impact of die assembly on TPV and predict its fatigue life. Fracture mechanics analysis is performed in order to correlate the stresses to critical defect size, and assess the impact of defects on TPV reliability and defect growth under thermal cycling.

3.1. TPV Stresses from Analytical modeling and FEM Analysis

Copper-plated cylindrical TPV in glass resembles a similar problem as elastic reinforcement fibers in ceramics and TSVs in silicon wafers. Therefore, a similar approach can be taken to analyze the stress fields around TPVs in glass. Thermal expansion mismatch between copper and glass induces thermal stresses in the surrounding glass. Depending on the size of inclusions and defects on TPV walls, these thermal stresses can lead to cracks in the glass. At high temperatures, copper tends to expand more than glass that creates radial compression and circumferential tension in glass. On the other hand, at cold temperatures, copper tends to shrink

more compared to glass, inducing radial tension and circumferential compression in glass. Stresses around a single cylindrical TPV in glass can be obtained by superposition of two problems sketched in Figure 3.2 assuming all materials are isotropic and linearly elastic [73].

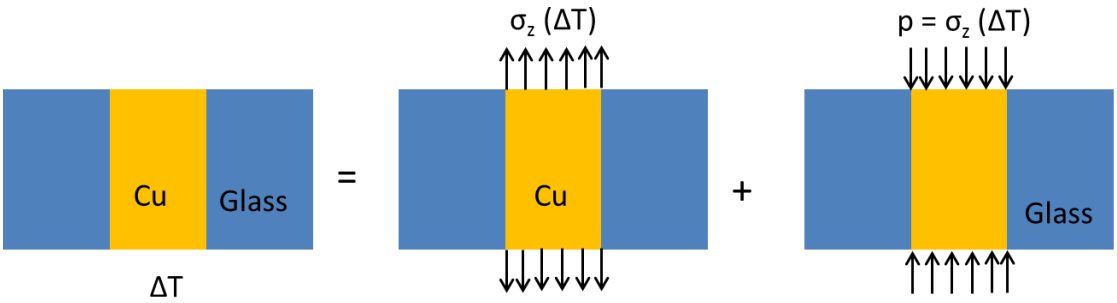


Figure 3.2. Original problem divided into superposition of two problems (a) original problem with a positive thermal load and traction-free surfaces, (b) Problem A with thermal load and surface tension (c) Problem B with only surface pressure with the same magnitude as in problem A [73].

In problem A, TPV is subjected to thermal loading as well as a mechanical tension at the ends. The fictitious stress was removed by superimposing problem B in which a stress of same magnitude is applied at both ends of TPV without thermal load. Lame's stress distribution with 2-D plane strain assumption is an analytical solution to Problem A which is commonly used for cylinder assemblies [74]. The stress in TPV copper region is uniform and triaxial, with the following components:

$$\sigma_r = \sigma_\theta = \frac{-E_{Cu}\varepsilon_T}{1-2\nu_{Cu}+\frac{(1+\nu_g)E_{Cu}}{(1+\nu_{Cu})E_g}} \tag{3.1}$$

$$\sigma_{z\theta} = \sigma_{r\theta} = \sigma_{rz} = 0 \tag{3.2}$$

$$\sigma_z = -\mathrm{E_{Cu}}\varepsilon_\mathrm{T}\left[\frac{1+\frac{(1+\mathrm{v_g})\mathrm{E_{Cu}}}{(1+\mathrm{v_{Cu}})\mathrm{E_g}}}{1-2\mathrm{v_{Cu}}+\frac{(1+\mathrm{v_g})\mathrm{E_{Cu}}}{(1+\mathrm{v_{Cu}})\mathrm{E_g}}}\right] \tag{3.3}$$

where $\sigma_\mathrm{r}, \sigma_\theta, \sigma_\mathrm{z}$ are radial, circumferential, and axial stresses and $\varepsilon_\mathrm{T} = (\alpha_\mathrm{Cu} - \alpha_\mathrm{g})\Delta\mathrm{T}$ is the CTE mismatch strain due to the thermal load ΔT respectively. The material properties, α, E, v, are the coefficient of thermal expansion (CTE), Young's modulus, and Poisson's ratio, with the subscripts Cu and g stand for the copper and glass, respectively. The corresponding stress fields in glass ($r > D/2$) is non-uniform and bi-axial [74]:

$$\sigma_\mathrm{r} = -\sigma_\theta = \frac{-\mathrm{E_{Cu}}\varepsilon_\mathrm{T}}{1-2\mathrm{v_{Cu}}+\frac{(1+\mathrm{v_g})\mathrm{E_{Cu}}}{(1+\mathrm{v_{Cu}})\mathrm{E_g}}}\left(\frac{\mathrm{D}}{2\mathrm{r}}\right)^2 \tag{3.4}$$

$$\sigma_\mathrm{z} = \sigma_{\mathrm{z}\theta} = \sigma_{\mathrm{r}\theta} = \sigma_{\mathrm{rz}} = 0 \tag{3.5}$$

where D is the diameter of TPV and r is the radial coordinate measured from the center of the TPV structure.

Equation 3.4 and 3.5 depict an axisymmetric stress distribution in the surrounding glass. The magnitude of radial and tangential stresses in glass diminishes quickly with square of the ratio between the radial distance r and diameter D , which implies that radial cracks initiating from the copper-glass interface should arrest in the glass. The maxima of radial and circumferential stresses occur at the boundary of TPV, and are independent of TPV diameter. Instead, the maximum stresses are mainly controlled by the thermal expansion mismatch and thermal load. Furthermore, axial stress $\sigma_\mathrm{z} = 0$ in glass implies that z-cracks are suppressed around an isolated TPV in an infinitely- thick glass. These 2-D solutions are valid under a plane-strain condition for an isolated infinitely long TPV.

The solution to Problem B is Boussinesq stress distribution commonly used in soil mechanics. This stress distribution due to the surface pressure is shown graphically in Figure 3.3

[75]. This stress distribution imposes high shear stress around TPV ends. These stresses arising in Problem B localize around the TPV ends and became negligible at a diameter distance away from the end of the TPV. Therefore, Lame's stress distribution can be used to calculate stresses and stress intensity factors in the glass around TPV far away from TPV ends, especially for high-aspect-ratio (height/diameter) TPVs embedded in a thick glass.

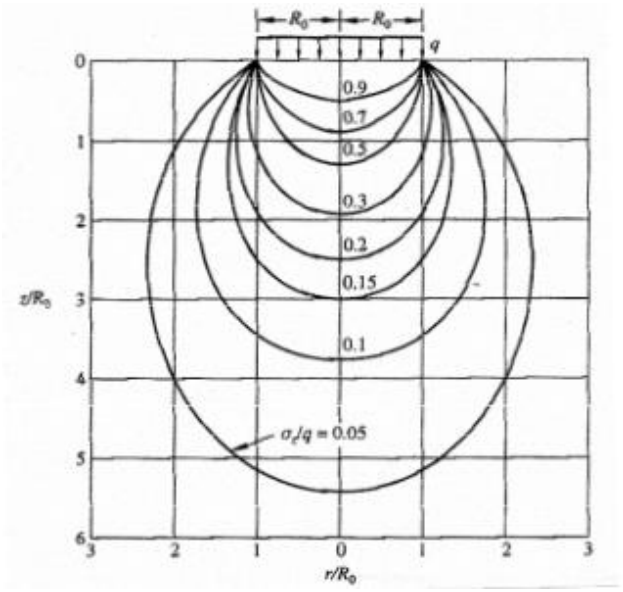


Figure 3.3. Boussinesq stress distribution due to surface pressure, solution to Problem B [76]

3.1.1. Verification with Finite Element Modeling

To investigate the validity of these assumptions for stress distribution, FEA simulations are performed on TPVs in glass with 300 μm thickness, 60 μm diameter, and 250^{o}C thermal load. Because of symmetry 1/4th of TPV was modelled using plane82 elements with axisymmetric option. Material properties are given in Table 1. Room temperature is assigned as the stress-free temperature for both copper and glass, similar to analytical equations.

Table 3.1 Material Properties

	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/^{o}C)
Glass	77	0.22	3.8
Copper	121	0.3	17.3

Figure 3.4 depicts the distribution of stresses in the fully-filled TPV structure. At the TPV ends, stress distribution approaches to 2-D plane strain condition. However, impacts from Boussinesq stress distribution become visible especially in shear stress that is localized around TPV ends.

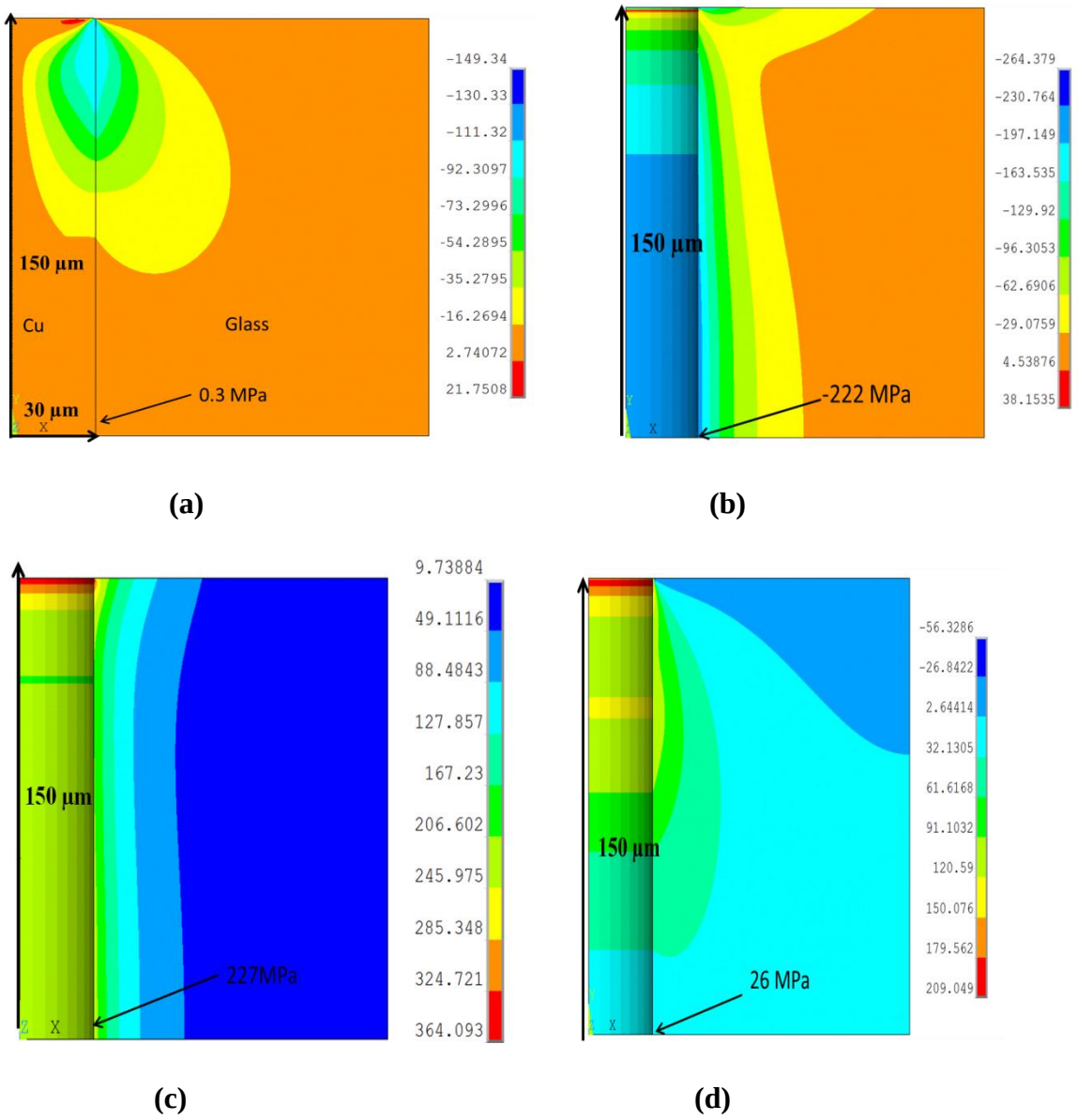


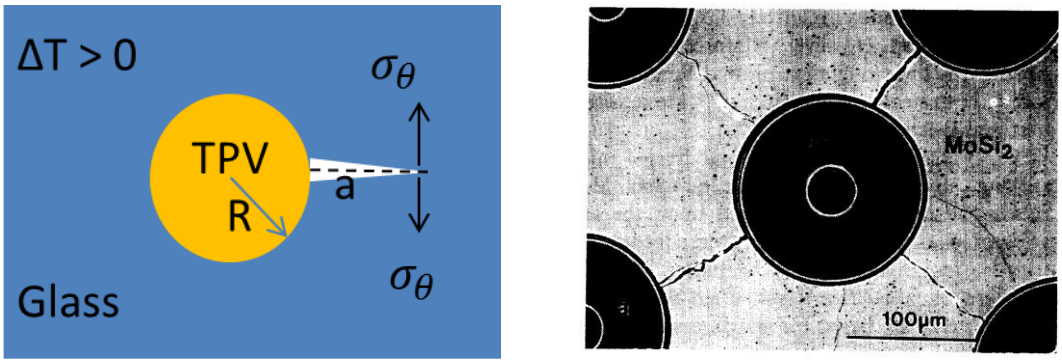
Figure 3.4. (a) Shear stress σ_{rz}, (b) Radial stress σ_r, (c) Circumferential stress σ_θ and (d) axial stress σ_z

According to the FEA results, a diameter away from TPV ends, radial and circumferential stress in glass is -222 MPa and 227 MPa respectively. Substituting the material properties in Equation 3.4, these stresses can be calculated as 218 MPa that matches the FEA results by 2%. Shear stress is 0.3 MPa and axial stress is 26 MPa that both should be 0 MPa according to Equation 3.5. This discrepancy can be explained by the effect of finite glass

thickness and TPV pitch that were assumed infinity in calculating the analytical stress distribution. However, it is seen that 2-D plane strain solutions can be used for predicting stresses approximately a diameter away from via ends and setting up conservative design constraints for reliability of TPV structures.

3.1.2. TPV-Induced Cracking

TPV-induced thermal stresses can drive glass cracking under a positive thermal load due to CTE mismatch between copper and glass. For positive thermal load, copper inside TPV expands more than the surrounding glass, which induces a tensile circumferential stresses σ_θ in glass. This stress can drive a radial crack, as shown in Figure 3.5. Using the analytical formulas from previous section, stress intensity factors can be estimated



(a) **(b)**

Figure 3.5. Illustration of TPV-induced radial glass cracking under a positive thermal load [77]

For fully-filled TPVs, the corresponding mode I stress intensity factor and energy release rate for the radial through-thickness crack is given by [77]:

$$K_I = \frac{-2E_{Cu}\,\Delta\alpha\,\Delta T}{1-2\nu_{Cu}+\frac{(1+\nu_g)E_{Cu}}{(1+\nu_{Cu})E_g}}\sqrt{R}\left(\frac{\pi}{8}\right)^{\frac{1}{2}}\left(\frac{a}{R}\right)^{\frac{1}{2}}\left(1+\frac{a}{R}\right)^{-3/2} \quad (3.6)$$

where a the initial radial is defect length extending from the edge of TPV and R is the radius of TPV. Stress intensity factor is plotted as a function of the crack length in Figure 3.6 for varying TPV diameters.

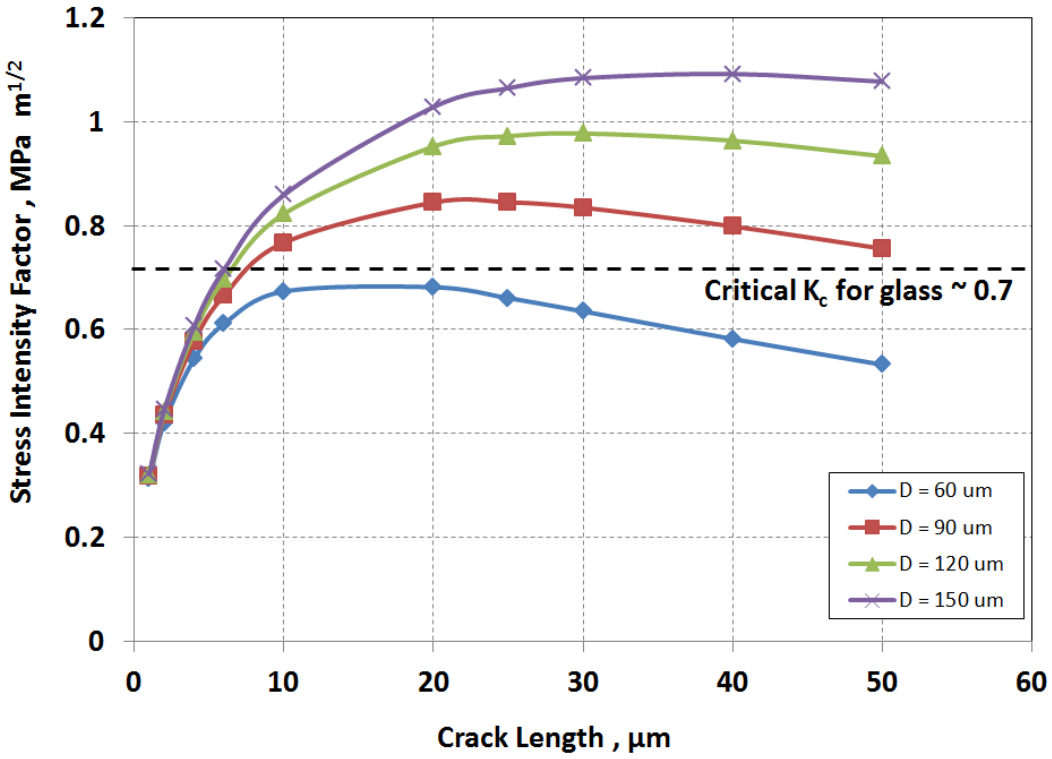


Figure 3.6. Variation of stress intensity factor with radial crack length and TPV diameter for a thermal load of ΔT=+250 ^{o}C

As shown in Figure 3.6, the driving force for TPV induced glass-cracking increases with diameter. The stress intensity factor at the radial defect initially increases with crack length, and then gradually reduces at a crack length greater than quarter of the diameter. This is due to the decaying stress on the crack tip according to Equation 3.4, as the distance of the crack tip to the center of TPV increases. Given the critical stress intensity factor of glass for brittle fracture as approximately 0.7 MPa $m^{1/2}$, the TPV induced glass cracking may not occur for diameters less

than 60 μm under a thermal load of 250°C. Glass cracking can be induced by a relatively large diameter fully-filled TPV with a long initial defect. However, the critical stress intensity factor for glass on TPV wall can be reduced by impact of via formation or interaction with water.

3.1.3. Annular TPV:

The annular TPV structure is an attractive solution to reduce the impact of the thermal mismatch on interfacial reliability by means of reducing the metal volume. With the traction-free boundary condition on the inner surface of the annular TPV, the stress distribution in via becomes non-uniform, different from that in a fully filled circular TPV. The 2-D solutions for the stress distribution in the annular TPV copper region are given by the following stress components [78]:

$$\sigma_r = \frac{-E_{Cu}\varepsilon_T}{1-2\nu_{Cu}+\gamma^2+(1-\gamma^2)\frac{(1+\nu_g)E_{Cu}}{(1+\nu_{Cu})E_g}}\left[1-\left(\frac{D_i}{2r}\right)^2\right], \tag{3.7}$$

$$\sigma_\theta = \frac{-E_{Cu}\varepsilon_T}{1-2\nu_{Cu}+\gamma^2+(1-\gamma^2)\frac{(1+\nu_g)E_{Cu}}{(1+\nu_{Cu})E_g}}\left[1+\left(\frac{D_i}{2r}\right)^2\right] \tag{3.8}$$

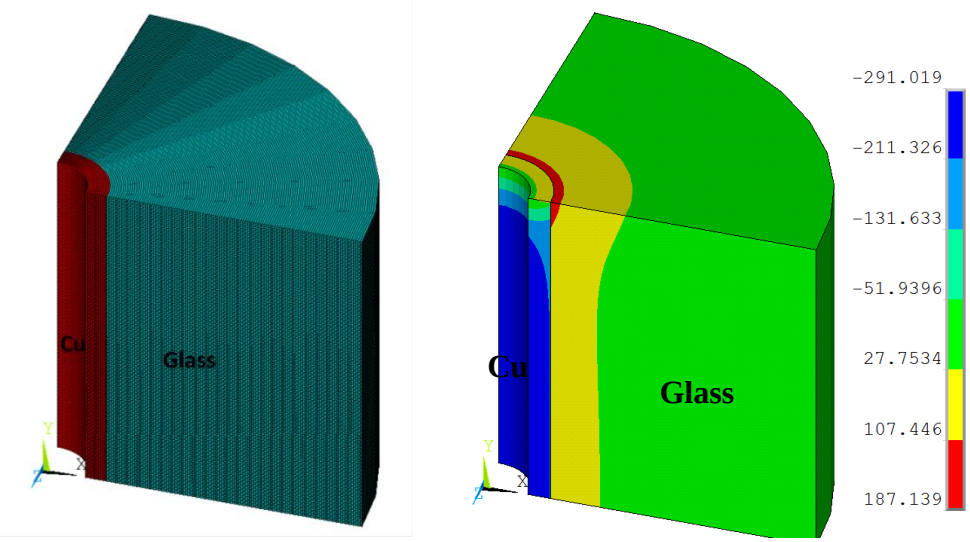
$$\sigma_z = \frac{-E_{Cu}\varepsilon_T}{1-2\nu_{Cu}+\gamma^2+(1-\gamma^2)\frac{(1+\nu_g)E_{Cu}}{(1+\nu_{Cu})E_g}}\left(1+\frac{(1+\nu_g)E_{Cu}}{(1+\nu_{Cu})E_g}\right) \tag{3.9}$$

where D_i is the inner diameter of the annular TPV and $\gamma = \frac{D_i}{D_{Cu}}$ is the diameter ratio. Correspondingly, the stress components in the glass are given as follows:

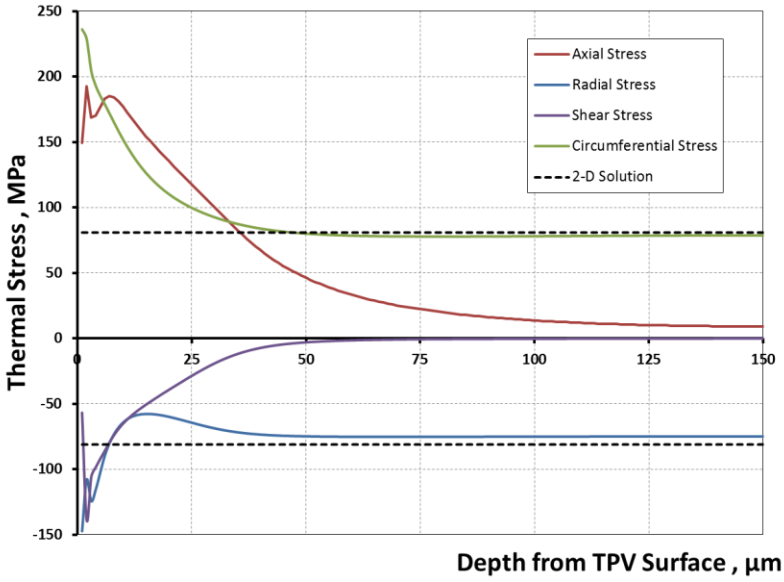
$$\sigma_r = -\sigma_\theta = \frac{-E_{Cu}\varepsilon_T(1-\gamma^2)}{1-2\nu_{Cu}+\gamma^2+(1-\gamma^2)\frac{(1+\nu_g)E_{Cu}}{(1+\nu_{Cu})E_g}}\left(\frac{D_{Cu}}{2r}\right)^2 \tag{3.10}$$

To verify these stress distributions, 2-D axisymmetric FEA model for an annular TPV with 10μm copper, 60 μm diameter in 300 μm thick glass was built and simulated with a thermal load of +150°C. The meshed model, contour plot of circumferential stress and variation of stress

along the depth of TPV is shown in Figure 3.7. As observed from Figure, the stress values away from surface for about a diameter approach to results based on equations.



(a) **(b)**



(c)

Figure 3.7.(a)1/4th V model (b) contour plot of circumferential stress (σ_Θ) and (c) Variation of thermal stress components in glass with respect to distance from TPV surface

According to equation 3.10, it is apparent that the magnitude of both radial and circumferential stresses in glass reduces with increasing D_i. As the diameter ratio, γ increases by increasing the inner diameter, the radial and shear stress are reduced compared to the fully filled TPV ($\gamma = 0$). Keeping the plated copper thickness constant (t_{Cu}) increasing the diameter brings down the diameter ratio ($\gamma = \frac{D_i}{D_{Cu}} = \frac{D_{Cu} - t_{Cu}}{D_{Cu}}$), thus leading to lower stress in glass. Therefore, for annular TPVs, in other words conformal plated TPVs, increasing diameter leads to reduced stress in glass surrounding the copper TPV. This trend is illustrated in Figure 3.8 by changing the diameter ratio with plated copper thickness.

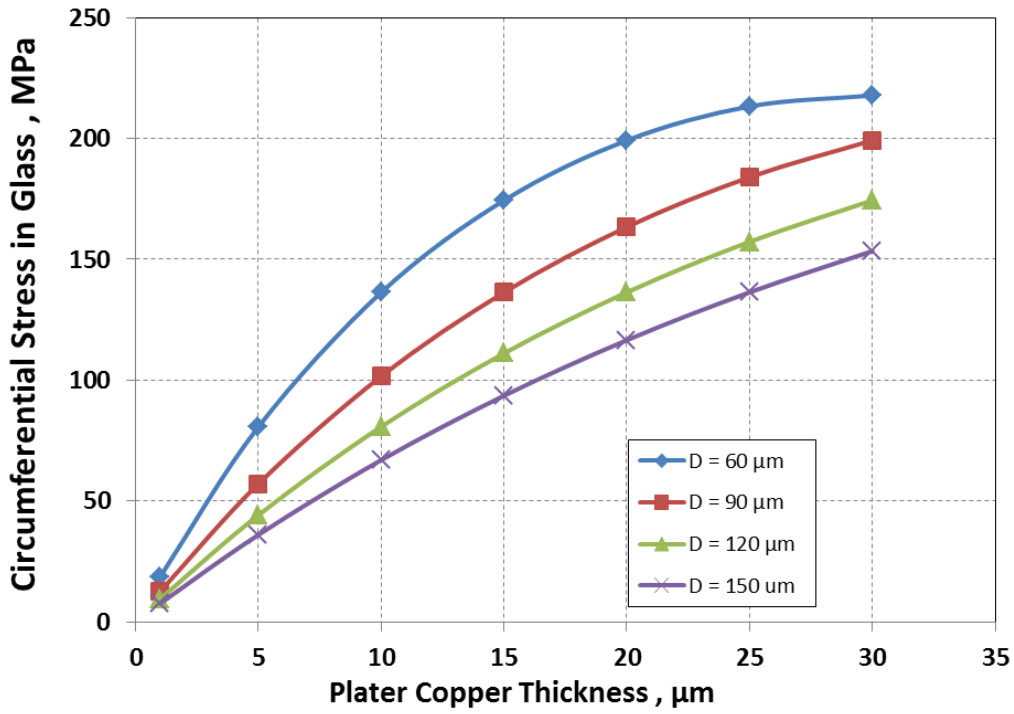


Figure 3.8. Variation of circumferential stress σ_θ with plated copper thickness for different TPV diameters

In Figure 3.9, relation of stress intensity factor for a radial crack to the maximum circumferential stress in glass/copper interface is plotted for a 10 µm radial defect. It is observed that, for TPVs with high diameters, it is possible to induce brittle glass fracture at lower stresses. However, TPVs with larger diameters require thicker copper to induce the same amount of stress on copper-glass interface as TPVs with smaller diameters.

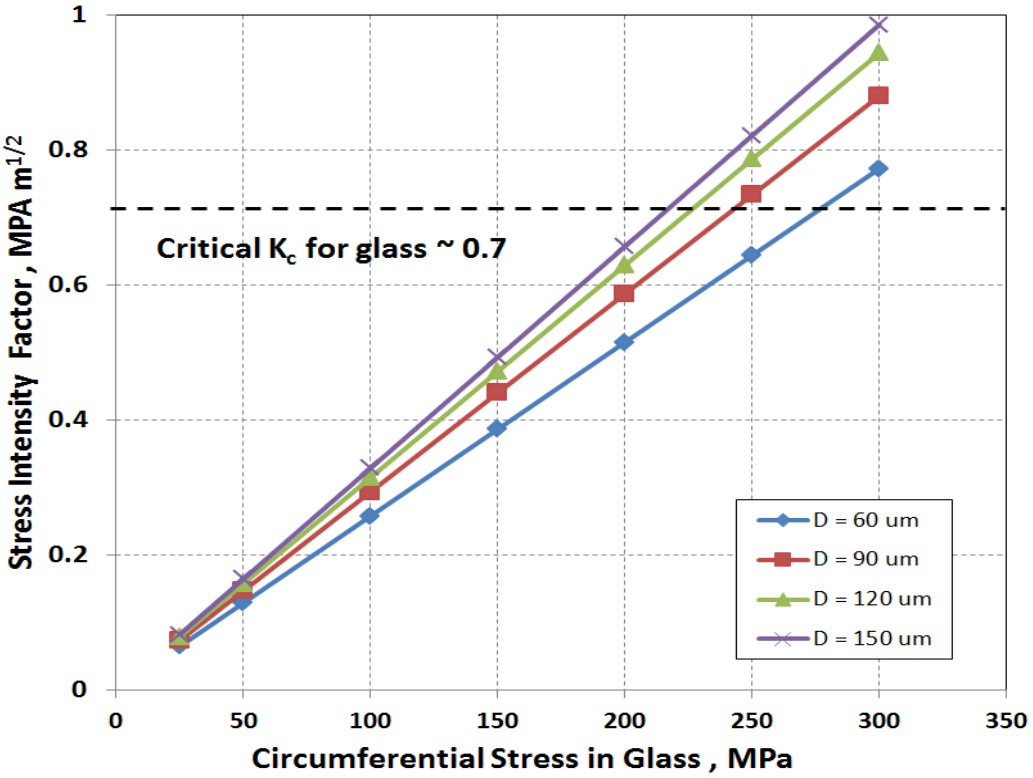


Figure 3.9. Change of stress intensity factor with maximum circumferential stress in glass for varying TPV diameters for a radial defect length of 10 µm.

3.1.4. Delamination of Copper along Via Wall:

Figure 3.10 depicts two modes of interfacial delamination for a conformal plated TPV structure. With a negative thermal load , the radial stress along the copper/glass interface is tensile. Consequently, the delamination crack can grow in a mixed peeling and shearing mode.

With a positive thermal load, the radial stress is compressive ,therefore interfacial rack can grow only in shearing mode. Therefore, delamination is more likely to occur at cold temperatures.

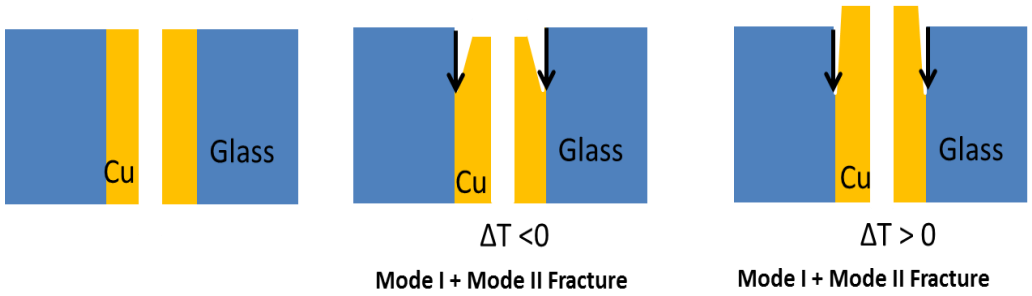


Figure 3.10. Illustration of interfacial delamination of copper from glass via wall under cooling and heating [79]

The crack driving force for a steady-state copper delamination from glass along the via sidewall has been derived for both the cooling and heating conditions. For an infinitely long TPV in an infinite glass with a semi-infinite circumferential crack along the copper/glass interface, energy release rate keeps increasing with crack length and reaches a steady state when the crack length is several times higher than the via diameter. The crack tip is far away from the glass surface so that the steady-state condition applies. This steady state value can be predicted analytically and can be used to set an upper bound for fracture driving force that may be used as a critical condition for conservative design of reliable TPV structures.

Given a thermal load, the steady-state energy release rate for the interfacial crack growth can be obtained by comparing the elastic strain energy far ahead of the crack front and that far behind the crack front. The energy release rate can be expressed as follows [80]:

$$G_{SS} = \frac{E_g \varepsilon_T^2 D_{Cu}}{4} \left(\frac{(1+\nu_{Cu})(1+\alpha_D)}{(1-2\nu_{Cu})(1-\alpha_D)+(1+\alpha_D)\frac{1+\nu_g}{1+\nu_{Cu}}} + \frac{1+\alpha_D}{2(1-\alpha_D)} \right) \quad \text{for } \Delta T < 0 \tag{3.11}$$

$$G_{SS} = \frac{E_g \varepsilon_T^2 D_{Cu}}{4} \left(\frac{(1+v_{Cu})(1+\alpha_D)}{(1-2v_{Cu})(1-\alpha_D)+(1+\alpha_D)\frac{1+v_g}{1+v_{Cu}}} + \frac{1+\alpha_D}{2(1-\alpha_D)} - \frac{1+\alpha_D}{(1-v_{Cu})(1-\alpha_D)+(1+v_g)(1+\alpha_D)} \right)$$

for $\Delta T > 0$ (3.12)

where $\varepsilon_T = (\alpha_{Cu} - \alpha_g)\Delta T$ is the thermal strain, and $\alpha_D = \frac{E'_{Cu} - E'_g}{E'_{Cu} + E'_g}$ is the first Dundur's parameter for elastic mismatch between copper and glass with $E' = \frac{E}{1-v^2}$. Equations 3.9 and 3.10 can be simplified by neglecting the elastic mismatch between glass and copper (i.e., $\alpha_D = 0$ and $v_g = v_{Cu} = v$) as follows [81]:

$$G_{SS} = \frac{E \varepsilon_T^2 D_{Cu}}{4(1-v)} \quad (3.13)$$

$$G_{SS} = \frac{E \varepsilon_T^2 D_{Cu}(1+v)}{8(1-v)} \quad (3.14)$$

For annular TPVs with a diameter ratio of $\gamma = \frac{D_i}{D_{Cu}}$, steady-state energy release rate Equations 3.13 and 3.14 are scaled by a factor of $(1 - \gamma^2)$, and becomes:

$$G_{SS} = \frac{E \varepsilon_T^2 D_{Cu}}{4(1-v)} (1 - \gamma^2) \text{ , at cooling} \quad (3.15)$$

$$G_{SS} = \frac{E \varepsilon_T^2 D_{Cu}(1+v)}{8(1-v)} (1 - \gamma^2) \text{ , at heating} \quad (3.16)$$

In Figure 3.11, variation of steady-state energy release rate for copper delamination along TPV sidewall is plotted with changing copper thickness for different TPV diameters. As expected, higher copper thicknesses lead to higher energy release rates, thus higher chance for crack growth. Furthermore, the energy release rate increases with TPV diameter. The critical energy release rate for delamination at copper-glass interfaces is not known as the TPV wall is a modified glass surface due to TPV formation. Roughness increases the mechanical adhesion of copper to glass TPV wall. Thus, a high energy release rate may be required to propagate delamination cracks. By equating the energy release rate with the interfacial adhesion energy, i.e.

G (a_c) = r, the critical crack length (a_c) may be determined, beyond that the delamination crack grows unstably. For a conservative design, one may require G_{ss}< r, so that all interfacial cracks remain stable under the prescribed thermal load.

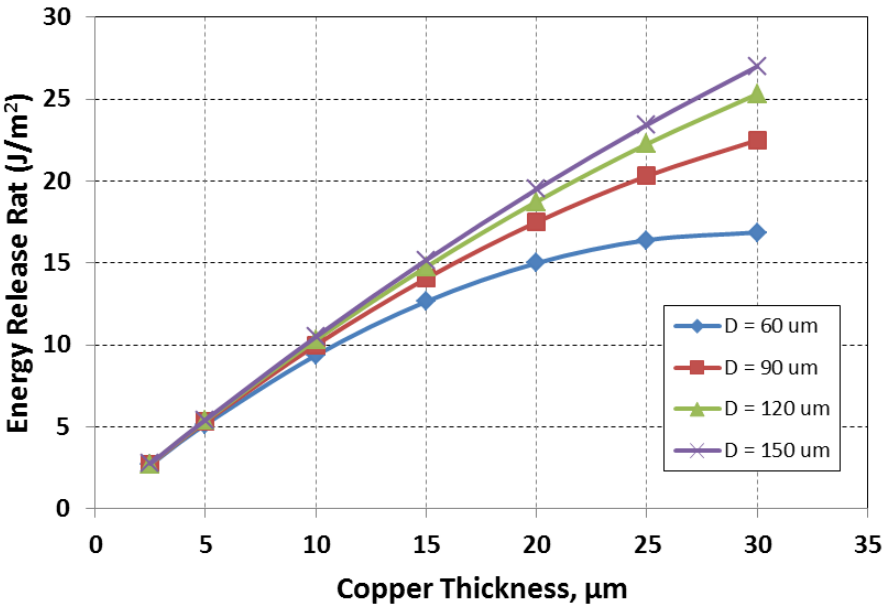
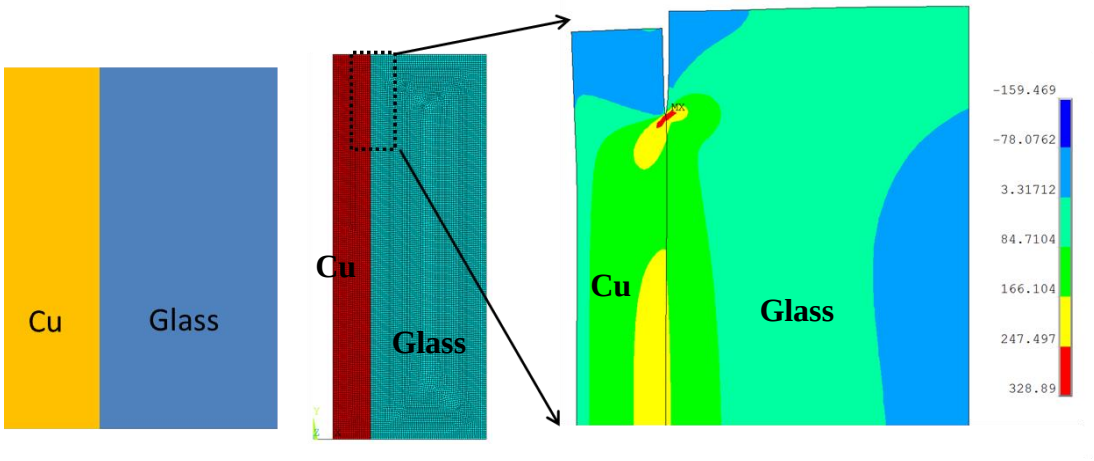


Figure 3.11. Variation of steady-state energy release rate for copper delamination with copper thickness and TPV diameter for a thermal load of ΔT= -250^{o}C

In order to verify the trend from analytical equations, 2-D axisymmetric finite element models were built with interfacial cracks between glass and copper. TPVs with 60 µm diameter in 200 µm glass were modeled and thickness of plated copper was varied. Figure 3.12 depicts the cross-section, the meshed finite element model and associated radial peeling stresses. A thermal load of -250 ^{o}C was applied and the energy release rate for interfacial crack propagation was calculated with J-integral method. At the crack tip, high peeling stress is observed as expected.



(a) **(b)** **(c)**

Figure 3.12. (a) Schematic cross-section, (b) meshed 1/4th TPV model and (c) distribution of peeling stress (σ_r), MPa

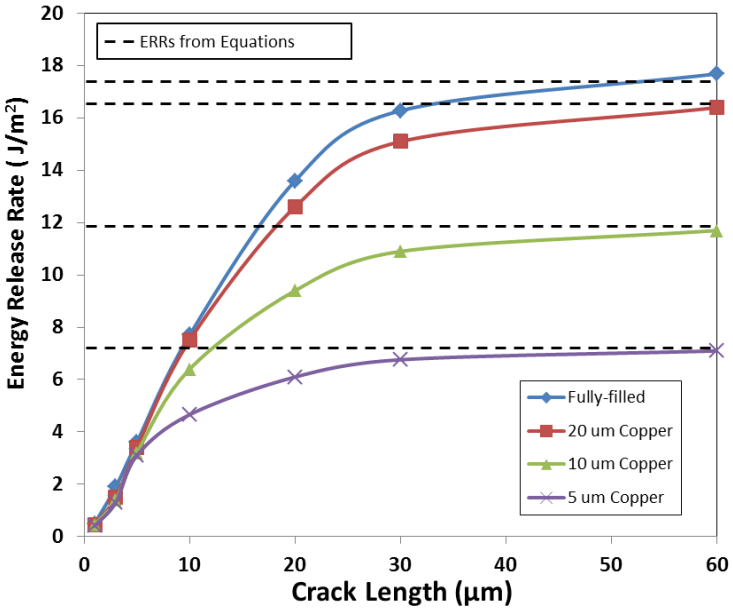


Figure 3.13. Variation of energy release rate with crack length for different copper thicknesses

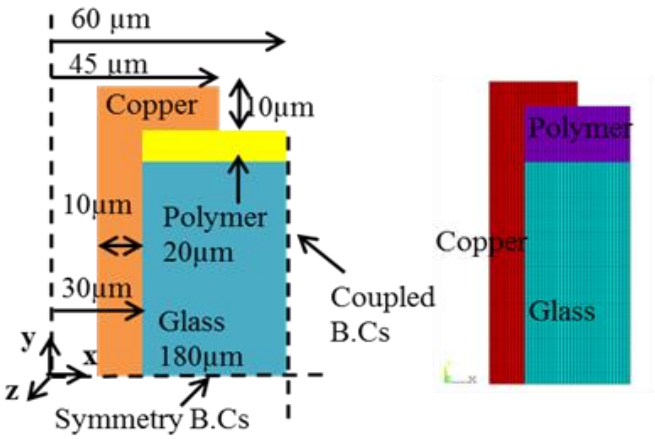
Variation of energy release rate with crack length for 60 um TPV is given in Figure 3.13 with varying plated copper thicknesses. As observed, the driving force for crack propagation

increases gradually with crack length up to approximately the steady state value given by analytical equations. Therefore, if the critical energy release rate for the copper/glass interface is engineered to the steady state value, then delamination failures are avoided. Also as expected, the energy release rates increase with higher copper thickness due to higher peeling forces.

This stress analysis based on 2-D plane-strain solution for high aspect ratio TPVs gives conservative design parameters for reliable structures. However impact of copper plasticity, varying stress-free temperature of materials and glass thickness were not taken into account. In order to take into account stress distribution near TPV ends along with impact of materials and geometry, finite element analysis needs to be performed using Ansys for TPV structures in various configurations.

3.2. TPVs in Polymer-Laminated Glass

Finite element modeling was performed using Ansoft Ansys to simulate stresses in and around the TPV structure in polymer-laminated glass. Parametric studies were performed to investigate the effect of geometric and material properties on stresses. A 2D axisymmetric model was built to analyze interfacial shear and first principal stresses due to thermal loading. Due to the symmetry of the structure, $1/4^{th}$ TPV was modeled as shown in Figure 3.14 along with boundary conditions and dimensions.



(a) **(b)**

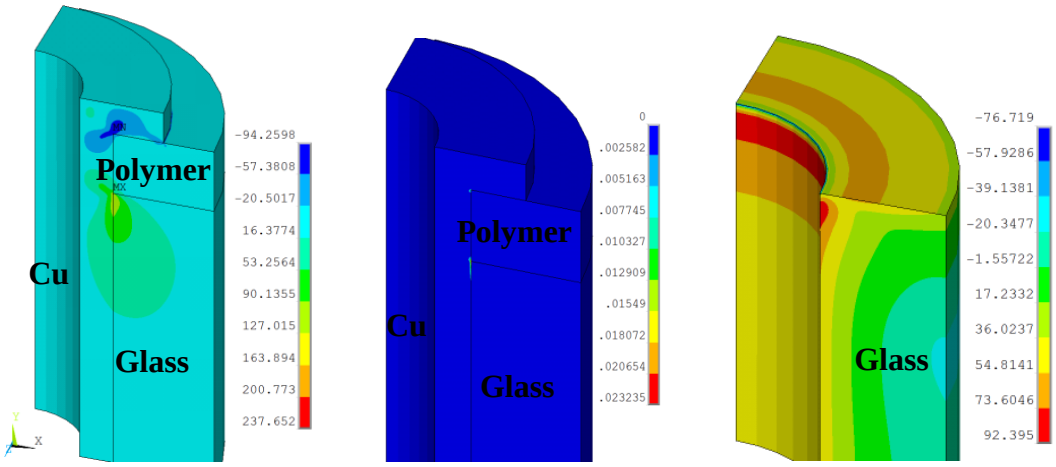
Figure 3.14. (a) Schematic of TPV used for mechanical modeling and parametric analysis, (b) meshed 1/4th TPV model

The material properties used in the simulations are given in Table 2. Two different types of glasses and polymers were used. All materials were assumed to be isotropic. Glass and polymer were modeled as linear elastic whereas bi-linear kinematic hardening model was used for copper with a yield stress of 172.38 MPa and tangent modulus of 1034 MPa. The structures were simulated to be heated to 125^{o}C and then cooled to -55^{o}C. As first process step is lamination of polymer on both sides of glass, glass transition temperature of the polymer was chosen as the stress free temperature for polymer-glass material system. For copper it was chosen as 108^{o}C [82].

Table 3.2 Material Properties Used in mechanical modeling

	Young's Modulus (GPa)	Poisson 's Ratio	CTE (ppm/^{o} C)	Stress free Temp. (^{o}C)
Glass	77	0.22	3.8	162
Polymer	6.9	0.3	31	162
Copper	Non-linear	0.3	17.3	108

At above the stress-free temperatures, expansion of copper creates radial compression and tangential tension in glass. On the other hand, at cold extremes, contraction of copper creates radial tension and tangential compression in glass. Polymer helps alleviate stresses around TPV ends at both temperature extremes. As glass is a brittle material, it is strong against compression but relatively weaker against tension. Therefore, maximum 1st principal stress was selected as a metric for crack failure in glass. Von Mises plastic strain in copper was considered as a metric leading to fatigue failure of copper. Shear stresses at material interfaces were considered as a metric to predict delamination failures. Simulation results corresponding to each failure metric are shown in Figure 3.15 and material junctions were observed to be critical regions.

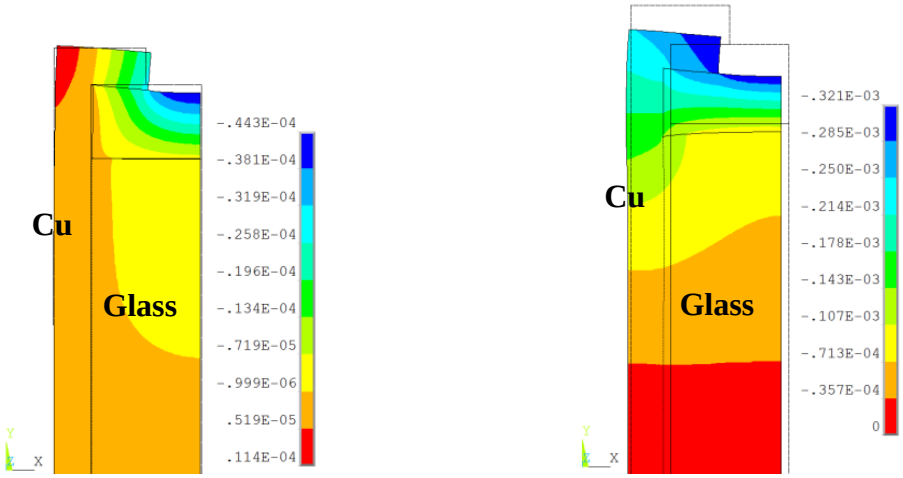


(a) **(b)** **(c)**

Figure 3.15. Distribution of (a) shear stress (σ_{xy}) (MPa), (b) Von Mises plastic strain in copper, and (c) 1st principal stress in glass (MPa) at -55^{o}C

Shear stresses are high at material junctions of copper-polymer and copper-polymer-glass that can initiate copper delamination through-via sidewall. Copper plastically deforms locally at TPV corners. Principal stress in glass is also high at TPV corner. Therefore, the probability of

cohesive cracks in glass is much higher around corner region compared to deep inside the via wall. Figure 3.16 shows the displacement of TPV regions along with the edges of undeformed model at hot and low temperature extremes. Copper sinking occurs at -55°C; however; copper expansion at 125°C is insignificant due to high stress-free temperature of polymer-glass assembly and annealed copper. Therefore, risk of damage on subsequent upper dielectric layers due to copper expansion is low.



(a) At 125°C **(b) At -55°C**

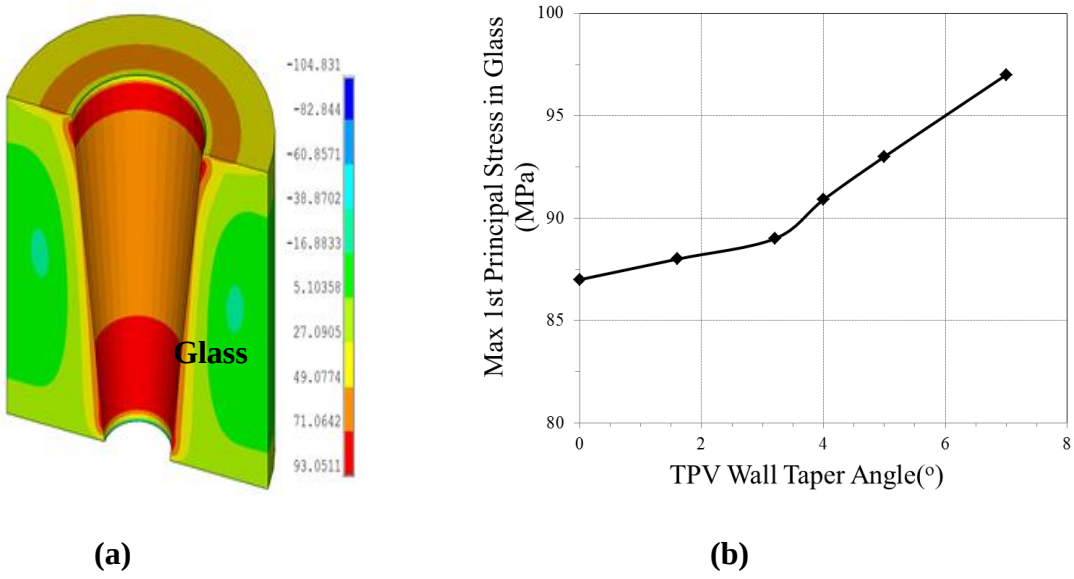
Figure 3.16. Displacement in y-direction (mm) magnified 50x (a) at hot and (b) at cold extreme

Some TPV formation options, such as ArF excimer laser ablation, leads to a tapered via with a difference in entrance and exit diameter. Taper angle can be defined as:

$$\theta = \tan^{-1}\left(\frac{D_{entrance}-D_{exit}}{2\times(H_{glass}+2\times H_{polymer})}\right) \quad (3.17)$$

$D_{entrance}$: TPV entry diameter
D_{exit} : TPV exit diameter
H_{glass} : Glass thickness
$H_{polymer}$: Polymer thickness

With ArF excimer laser drilling of 180 µm thick glass, for a laser entry diameter of 60 µm, exit diameter is around 40 µm that corresponds to a taper angle about 3^{o}.The contour plots of the 1^{st} principal stress in glass for the tapered and non-tapered TPV are shown in Figure 3.17.



(a) **(b)**

Figure 3.17. (a) Distribution of 1^{st} Principal stress (MPa) in glass with 60 µm TPV with taper, (b) variation with taper angle

Decreasing the exit diameter of TPV leads to higher taper in TPV wall and higher stresses around the smaller diameter. Change of maximum 1^{st} principal stress in glass with TPV wall taper angle is given in Figure 3.15. From reliability standpoint, taper in TPV formation should be kept as low as possible. However, taper of TPV does not lead to dramatic change in stress distribution. Therefore, for parametric studies, quarter TPV model can be used.

3.2.1. Effect of Aspect Ratio

Parametric studies are performed with varying TPV diameter and glass thickness, while keeping the polymer and conformal plated copper thicknesses constant. As shown in Figure 3.18, maximum 1st principal stress in glass slightly decreases with increasing diameter. For the same TPV diameter, increasing aspect ratio induces higher stress and plastic strain, but impact of glass thickness becomes insignificant beyond an aspect ratio of 3.

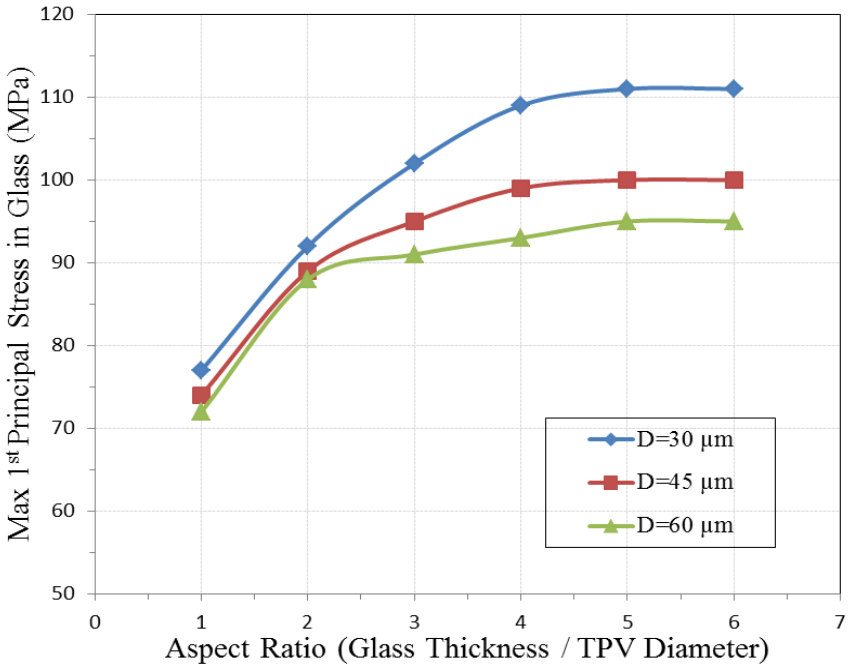


Figure 3.18. Variation of maximum 1st principal stress on glass, MPa with aspect ratio

Therefore, using thinner glass panels is preferred from reliability stand point. Furthermore, via formation becomes faster with decreasing glass thickness. However; challenges in glass-handling may compromise the overall reliability with the reduction of glass thickness.

3.2.2. Effect of Material Properties:

Impact of glass and polymer CTE on maximum glass stress is summarized in Figure 3.19. Stress on glass decreases with reduction in CTE mismatch between polymer and glass. Therefore, for lower TPV stresses, glasses with higher CTE and polymers with lower CTE should be preferred.

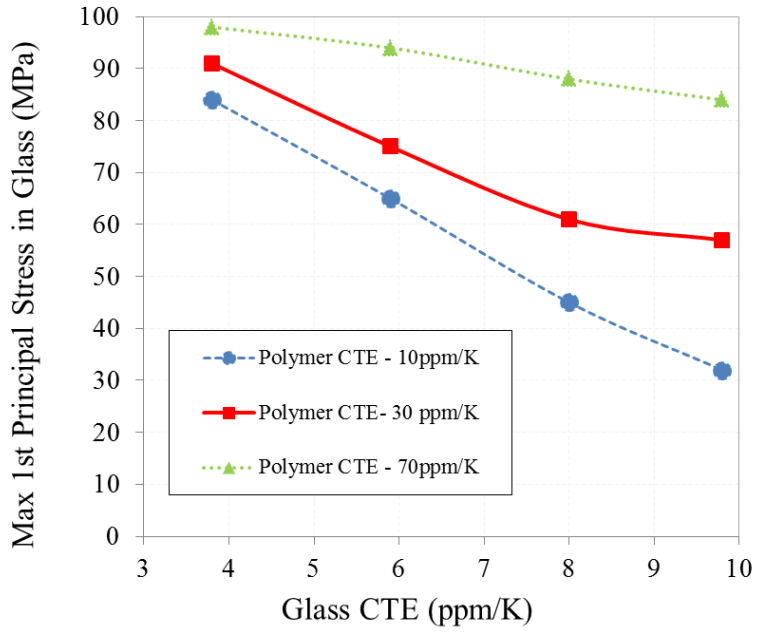
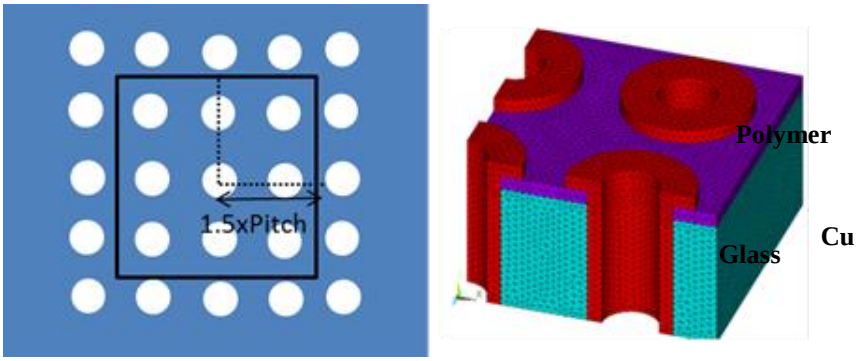


Figure 3.19. Variation of stress with CTE of polymer and glass

3.2.3. Effect of TPV Pitch

To capture the impact of neighboring TPVs, 3D TPV models are built according to the unit cell shown in Figure 3.20. A quarter-symmetric structure is modeled with symmetric boundary conditions on inner surfaces, and periodic boundary conditions on outer surfaces.



(a) **(b)**

Figure 3.20. Finite element analysis for evaluating the impact of TPV pitch: (a) Unit cell used for modeling and (b) meshed model of 1/8th TPV with neighboring vias

The contour plot of 1st principal stress in glass at 125^{o}C is shown in Figure 3.21. It is observed that stresses are localized around the vicinity of TPVs, while stresses in between TPVs are much smaller.

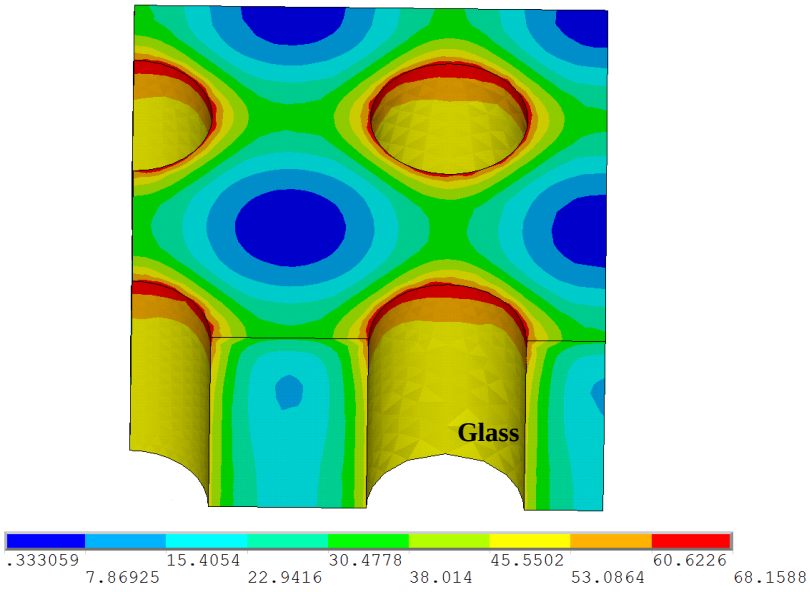


Figure 3.21. Distribution of 1st Principal Stress in glass, MPa, at 125^{o}C

Parametric studies are performed by varying the TPV pitch while keeping other parameters and copper thickness constant. Figure 3.22 shows that the impact of neighboring TPVs on maximum 1st principal stress in glass is subtle and becomes insignificant for TPV pitches higher than 1.5 TPV diameters.

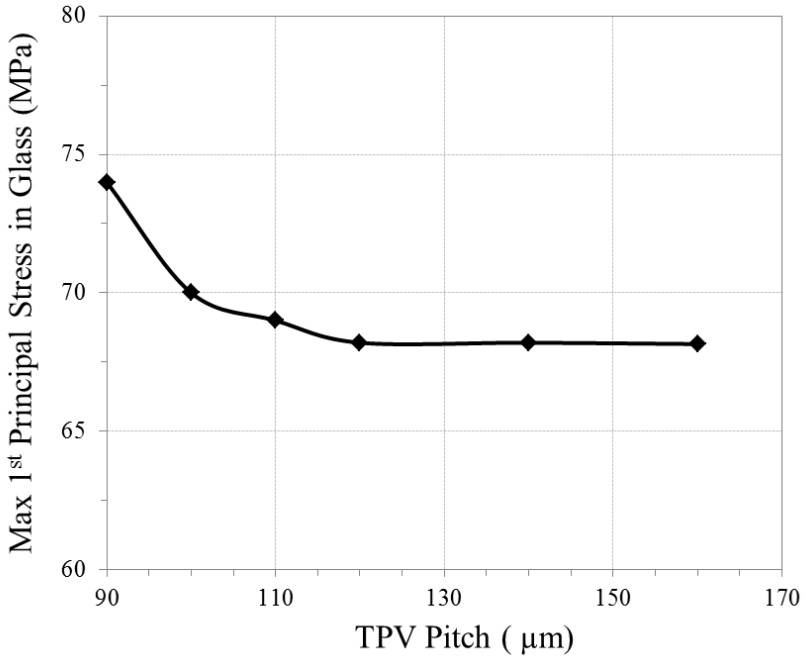
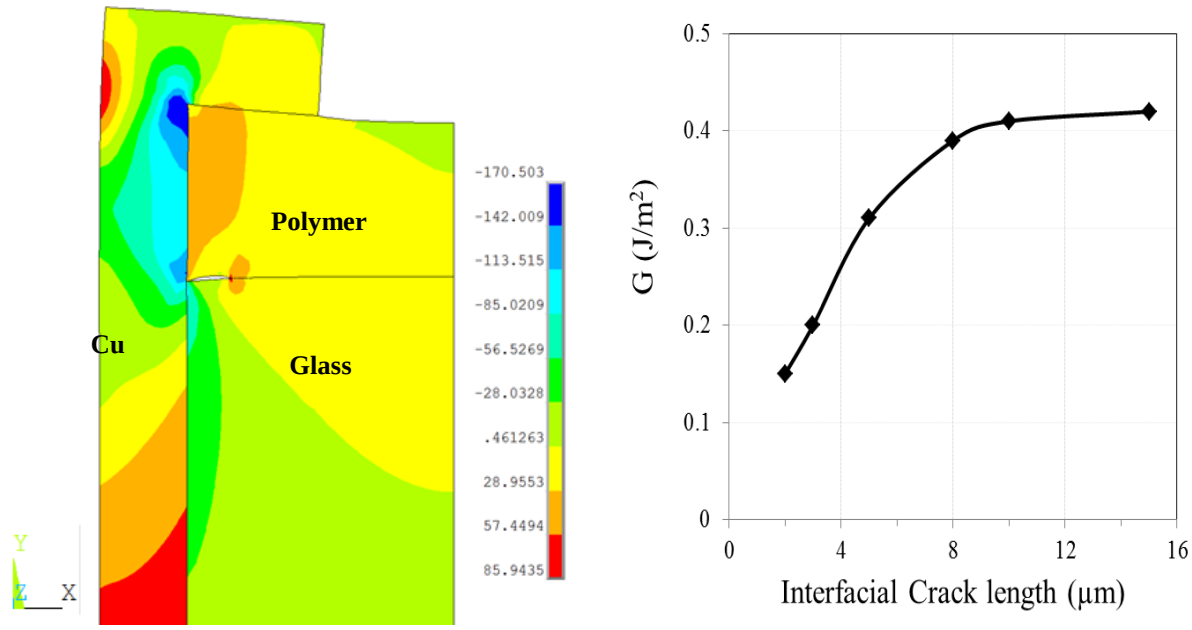


Figure 3.22. Variation of maximum 1st principal stress in glass as a function of via diameter and pitch

For TPVs fabricated in this study, via pitch is two times the diameter. Therefore, the impact of neighbor TPVs are negligible. Furthermore, due to double–sided fabrication processes and symmetry, there is no warpage in glass panel that can impose a global displacement on TPV. Therefore, chance of failure can be assumed identical for all TPVs independent of location on the glass panel in this study.

3.2.3. Effect of Polymer-Glass Delamination

Via formation by laser ablation process on polymer-laminated glass can create delamination of polymer from glass, especially around the exit region. In order to assess the behavior of this interfacial crack during thermal cycling, predefined interfacial cracks were built in the 2D model. Associated energy release rate for the interfacial crack (G) is calculated using J-integral method for linear elastic condition.



(a) **(b)**

Figure 3.23. (a) Contour plot for σ_y, MPa and (b) variation of energy release rate with crack length

As seen in Figure 3.23, there is high stress in y-direction (σ_y) that tends to open the crack at -55^{o}C with increasing energy release rate. However, computed G values are significantly lower than the debonding energy of polymer/glass interface that may increase up to 10 J/m^2 with

adhesion promoting processes. At 125 ^{o}C, G values for interfacial crack are significantly lower due to high stress-free temperatures of the material system. Therefore, growth of polymer/glass interfacial crack during thermal cycling is unlikely for annular TPVs.

3.2.4. Fatigue Life of TPV

As the simulations show, CTE mismatch between copper, glass and polymer leads to plastic deformation in copper during thermal cycling. This plastic deformation along with elastic strain may lead to fatigue failure of TPVs. The fatigue life of TPVs for different materials can be predicted using Coffin-Manson type of Cu fatigue model equation [83]:

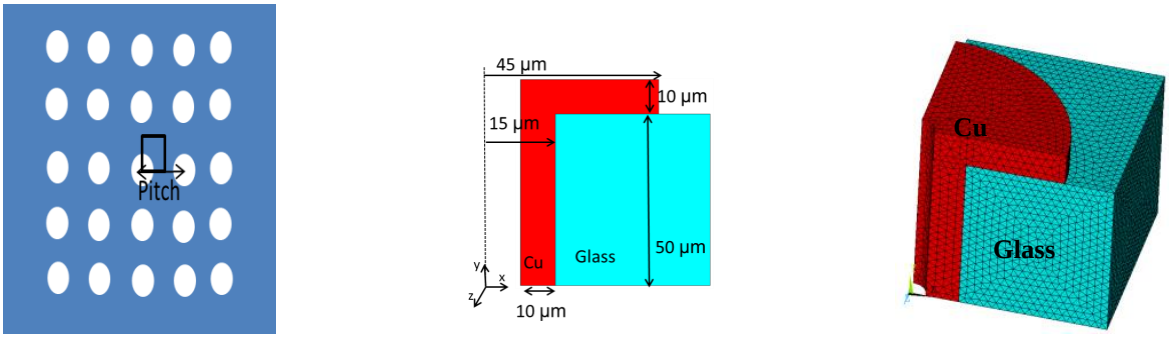
$$N_f^{-0.6} \times \varepsilon_f^{0.75} + \frac{0.9}{E}\sigma \left[\frac{e^{\varepsilon_f}}{0.36}\right]^{0.1785\ log_{10}\left[\frac{10^5}{N_f}\right]} = \Delta\varepsilon \tag{3.18}$$

where N_f, $\varepsilon_f = 0.3$, σ=220 MPa , E and $\Delta\varepsilon$ are the number of cycles to failure, fatigue ductility coefficient of copper, tensile strength of copper, elastic modulus of copper and total strain range respectively. For the TPV model shown in Figure 3.12, plastic strain range per cycle is obtained from simulations. Using this strain value, fatigue life is predicted from Equation 3.18. TPV fatigue life of 14000 thermal cycles is predicted and fatigue life is mainly limited by the polymer selection. This fatigue life estimation is only approximate as the actual mechanical properties of electroplated copper are not measured for the fabricated test samples. However, these calculations still can provide insight into design of TPVs for reliability. Also, it shows that copper fatigue failure is very unlikely to occur in glass TPVs.

3.3. TPVs in Bare Glass

Having a polymer film on glass surface limits the available options for making smaller

vias. Therefore, there is a need to study vias in bare glass interposers. by simulating the thermomechanical stresses and strains inside and surrounding the TPV structures in glass. In order to predict the intensity and distribution of these stresses, 3D models of TPVs were built as shown in Figure 3.22. Due to the symmetry of the structure, each via model is $1/8^{th}$ of the actual TPV. As TPVs are distributed periodically in an array, a square with each side being half of the TPV pitch was chosen as a unit cell for modeling. Symmetry boundary conditions were applied on two inner surfaces of the models, while coupled boundary conditions were applied on two outer surfaces of the unit cell to mimic the periodic layout. The schematic cross-section with geometry values is also presented in Figure 3.24.



(a) **(b)** **(c)**

Figure 3.24. (a) Unit cell used for modeling ,(b) schematic cross-sectional drawing of modeled TPV and (c) 3D meshed model of $1/8^{th}$ TPV.

The material properties used in the simulations are given in Table 3. All materials were assumed to be isotropic. Glass was modeled as linear elastic, whereas bi-linear kinematic hardening model was used for copper with yield strength of 172.3 MPa and hardening modulus of 1034 MPa. Effect of very thin Ti adhesion layer was neglected. A standard thermal load cycle

of -55^{o}C to 125^{o}C was used in the analysis with a dwell-time of 15 min at both extreme temperatures.

Table 3.3 Material Properties Used in mechanical modeling

	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/^{o} C)	Stress free Temp. (^{o}C)
Glass	63	0.23	3.17	50
Copper	121	0.3	17.7	50

When the system is heated to 125 ^{o}C, copper tends to pump out due to its high CTE compared to glass. Expansion of copper creates radial compression and tangential tension in glass. Compressive axial stresses are developed at the center of the copper. Furthermore, high shear stress and 1st principal stress were observed at the top edge of the glass, which might create delamination or cracks in glass. The contour plots of the mentioned strains and stresses are shown in Figure 3.25.

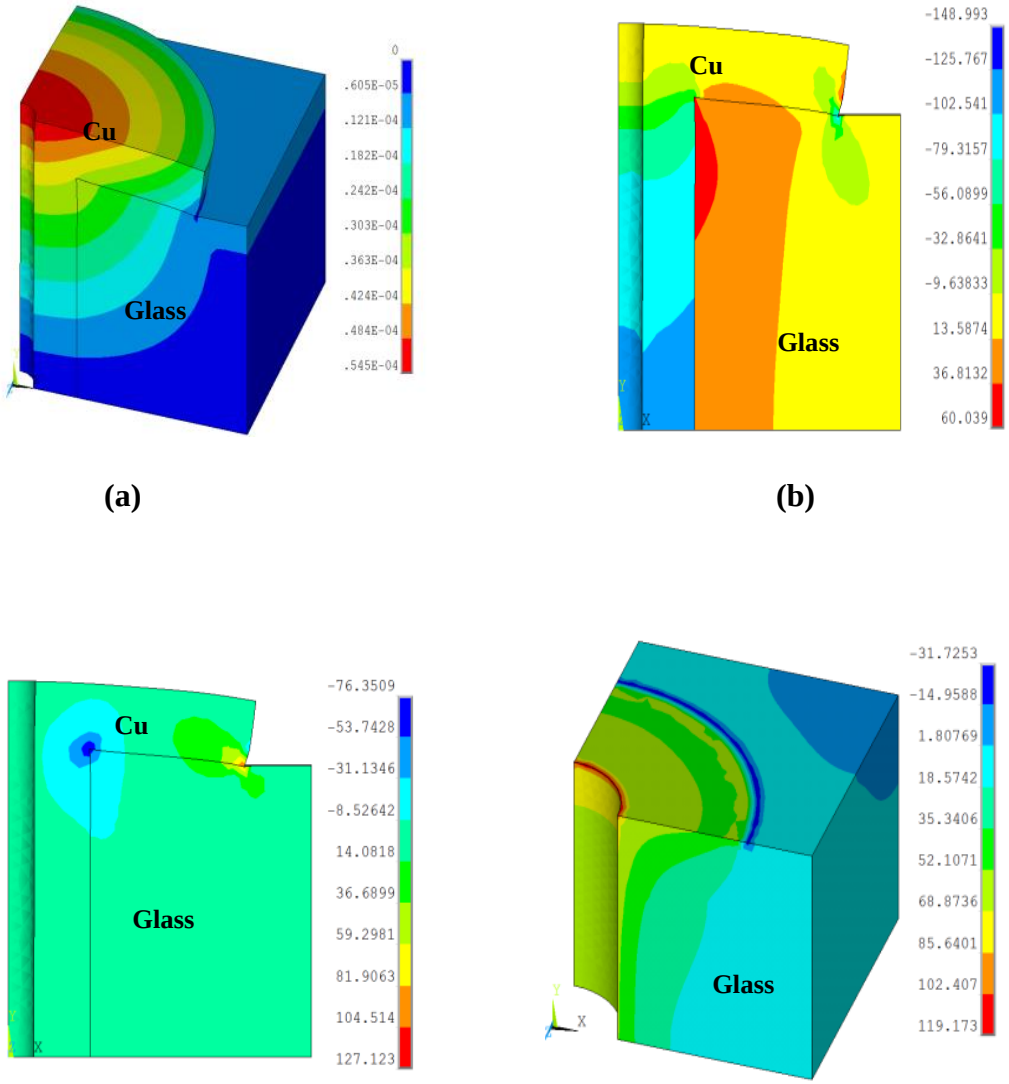
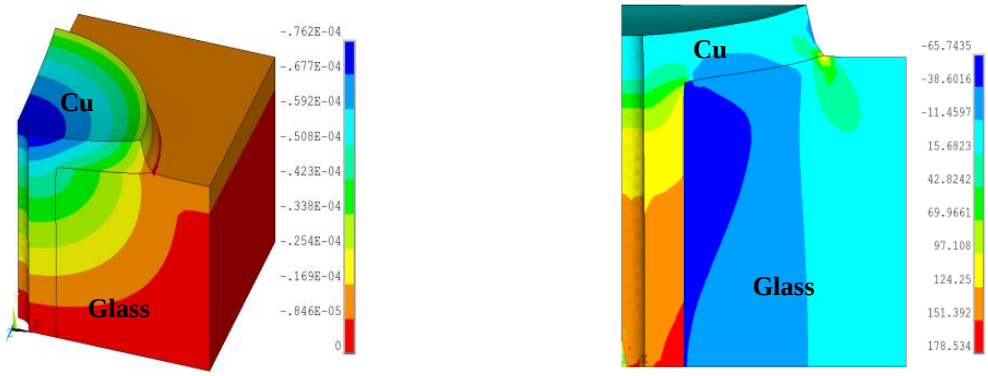


Figure 3.25 Contour plots for the (a) axial displacement, mm (b) axial stress, MPa (c) shear stress, MPa and (d) 1st principal stress at 125°C

When the system is cooled down to -55°C, contraction of copper creates radial tension and tangential compression in glass. High tensile stress occurs in copper core due to lower CTE glass around it. The contour plots at cold extremes are shown in Figure 3.26. Large shear stress and tensile peel stress in radial direction increases chance of interfacial delamination at cold

extremes. Plastic deformation of copper occurs in a limited region around the corner.



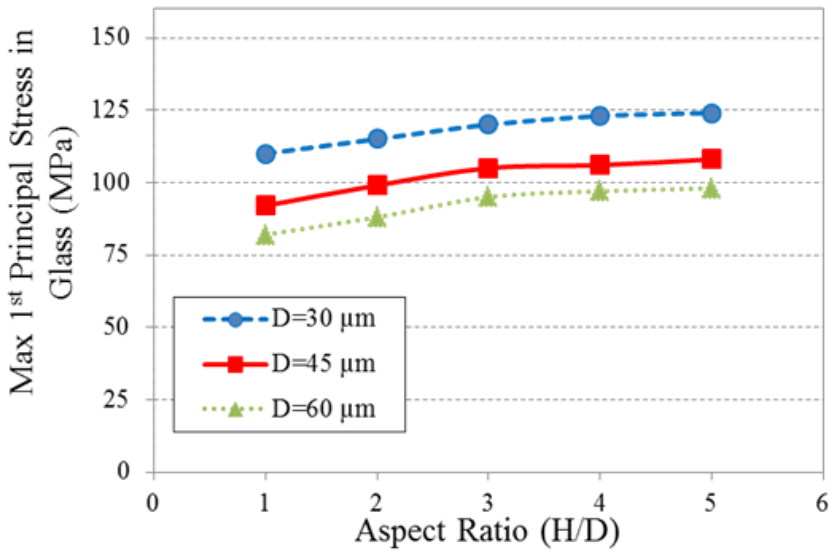
(a) **(b)**

Figure 3.26. Contour plots for the (a) axial displacement, mm (b) axial stress, MPa at -55^{o}C

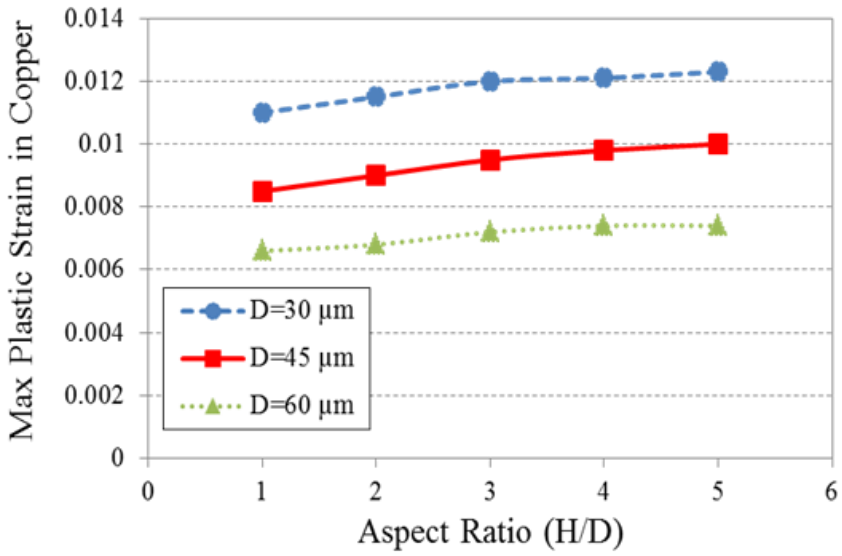
This stress-strain analysis provides a general view of possible failure locations. According to this analysis, delamination of copper and cracking of glass around TPV corner might be of concern.

3.3.1 Effect of Aspect Ratio

Parametric studies are performed with varying TPV diameter and glass thickness. This analysis can provide important guidelines for the reliability of TPVs. As glass is brittle, maximum 1st principal stress in glass is selected as the metric for crack formation. Maximum von Mises plastic strain in copper is chosen as a metric for fatigue failure in copper. TPV pitch and conformal copper thickness is kept constant at 120 µm and 10 µm respectively.



(a)



(b)

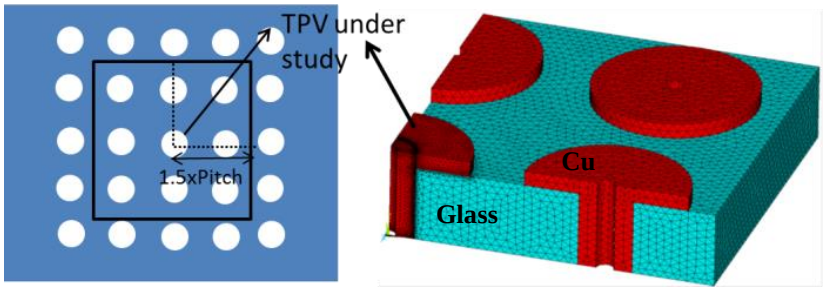
Figure 3.27. Impact of aspect ratio (H/D) on (a) 1st principal stress and (b) equivalent plastic strain TPV stress at 125°C

As shown in Figure 3.27, for a given aspect ratio, both maximum 1st principal stress in glass and von Mises plastic strain in copper decreases with increasing diameter. As the plated

copper thickness is kept constant, increasing diameter reduces the copper percentage in a square unit cell that reduces the impact of CTE mismatch. For TPVs with same diameter, increasing aspect ratio leads to higher principal stress and plastic strain; however, stresses stabilize with the aspect ratio. This can be explained through free-edge effect. Free-edge effects are present through a depth of two TPV diameters, and thus, with increasing aspect ratio, the edge effect disappears.

3.3.2 Effect of Pitch

In order to analyze impact of pitch, unit cell in Fig.3.22 is enlarged in order to contain the neighboring vias, as illustrated in Figure 3.28. A quarter-symmetric structure is modeled with symmetric boundary conditions on inner surfaces, and periodic boundary conditions on outer surfaces. Dimensions of TPV were chosen identical to the one shown in Figure 3.24.



(a) **(b)**

Figure 3.28. Finite element analysis for evaluating the impact of TPV pitch: (a) Unit cell used for modeling and (b) meshed model of 1/8th TPV with neighboring vias

The contour plot of 1st principal stress in glass at 125 ^{o}C is shown in Figure 3.29. It is observed that stresses are localized around TPVs whereas stresses in between TPVs are comparatively smaller.

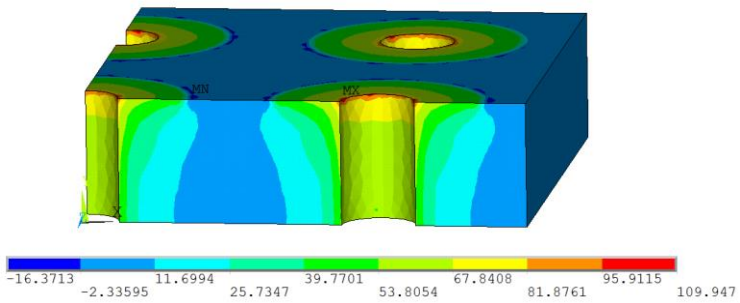


Figure 3.29. Distribution of 1st Principal Stress in glass, MPa, at 125°C

Parametric studies are performed by varying the TPV pitch and diameter while keeping the thickness of glass and plated copper constant. Figure 3.30 shows that the impact of neighboring TPVs on maximum 1st principal stress in glass is not significant for TPV pitches higher than 2 TPV diameters.

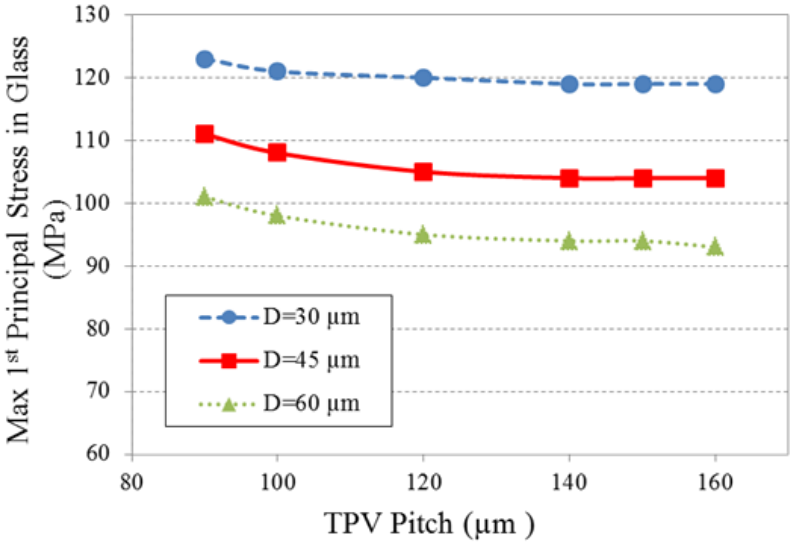


Figure 3.30. Variation of maximum 1st principal stress in glass as a function of via diameter and pitch

For TPVs fabricated in this study, via pitch is four times the diameter. Therefore, the impact of neighbor TPVs are negligible. Furthermore, due to double–sided fabrication processes and high dimensional stability of glass, there is no significant warpage in glass panel that can

impose a global displacement on TPV. The probability of failure is identical for all TPVs, independent of their location on the glass panel.

3.3.3. Fatigue Life of TPVs

During thermal cycling, larger CTE mismatch between copper and glass creates strains in copper. Total strain range in copper per thermal cycle is the summation of elastic strain range and plastic strain range that the TPV experiences during temperature cycling, and is an important parameter for identifying the fatigue life of TPV. . Using total strain range per cycle, the fatigue life of TPVs in bare glass is predicted by numerically solving Coffin-Manson equation with Engelmaier's Model [83].

$$N_f^{-0.6} \times \varepsilon_f^{0.75} + \frac{0.9}{E}\sigma \left[\frac{e^{\varepsilon_f}}{0.36}\right]^{0.1785 \log_{10}\left[\frac{10^5}{N_f}\right]} = \Delta\varepsilon \qquad (3.19)$$

ε_f : Fatigue ductility coefficient of copper (0.15)

N_f : Number of cycles to failure

$\Delta\varepsilon$: Total Strain Range

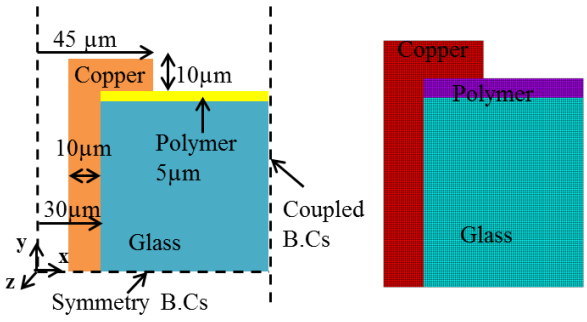
E : Young's modulus

σ : Ultimate tensile strength (220 MPa)

For a TPV of 30 µm diameter on 100 µm thick glass with 10µm of plated copper, maximum strain range is approximately 0.0045, corresponding to a fatigue life of above 8000 thermal cycles. This fatigue life estimation is subjected to errors as the mechanical properties of electroplated copper, such as its ductility or strength are not measured with electroplated copper samples, but instead taken from literature. However, the results indicate that fatigue failure of copper is unlikely with TPVs in glass.

3.4. TPV Stresses with via-first process

TPV stresses are sensitive to not only the structure but also the process flow that determines the thermal load on the structure. This section models the thermomechanical characteristics of the TPV structures in glass fabricated from via-first process. The structure consists of three different materials with varying CTEs that are bonded together. This bonding constrains the free thermal expansion and contraction of materials, leading to thermomechanical stresses that raise reliability concerns. To capture the fabrication-induced stress, different materials were sequentially activated using element birth/death approach in Ansys in accordance with the actual fabrication steps and process temperatures. A 2-D axisymmetric model was built to analyze interfacial shear stress and 1st principal stresses. Parametric studies were also performed with different polymer thicknesses. The schematic cross-section (1/4th via) is shown in Figure 3.31 along with boundary conditions and geometric dimensions. Symmetry boundary condition is applied on inner surface of the model, while coupled boundary conditions are applied on outer surface of the via to mimic the periodic layout.



(a) **(b)**

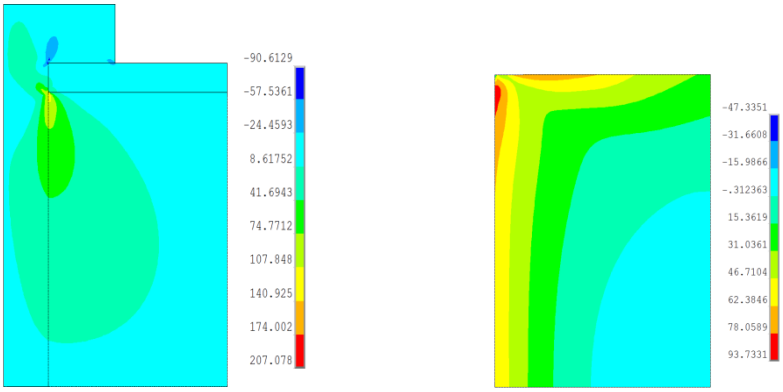
Figure 3.31. (a) Schematic cross-section of TPV used for mechanical modeling and parametric analysis, (b) meshed 1/4th TPV model

The material properties used in the simulations are compiled in Table 3.4. All materials were assumed to be isotropic. Glass and polymer were modeled as linear elastic, whereas bilinear kinematic hardening model was used for copper with yield strength of 172.3 MPa and hardening modulus of 1034 MPa. A standard thermal load cycle of -55^{o}C to 125^{o}C was used in the analysis with a dwell time of 15 min at both extreme temperatures. As the first process step is lamination of polymer on both sides of glass, glass transition temperature of the polymer was chosen as the stress-free temperature for polymer-glass material system. For copper it was chosen as 108 ^{o}C.

Table 3.4 Material Properties Used in mechanical modeling

	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/^{o}C)	Stress free Temp. (^{o}C)
Glass	63.6	0.23	3.17	162
Copper	121	0.3	17.3	108
Polymer	5	0.3	39	162

The contour plots of the 1st principal stress in glass and shear stress are shown in Figure 3.32. Due to CTE mismatch, stress localization occurs at the interfaces of materials. High shear stresses at the corners of TPV and landing pads can drive delamination failures. High 1st principal stress in glass around TPV corner raises chances for crack-formation in glass around TPV entrance sites compared to other locations.



(a) **(b)**

Figure 3.32. Contour plots for the (a) shear stress, MPa and (b) 1st principal stress, MPa in glass at -55°C

TPV formation by electrical discharge process results in a tapered via with a difference in entrance and exit diameter. Taper angle can be defined as:

$$\theta = \tan^{-1}\left(\frac{D_{entrance}-D_{exit}}{2\times(H_{glass}+2\times H_{polymer})}\right) \quad (3.20)$$

$D_{entrance}$: TPV entry diameter

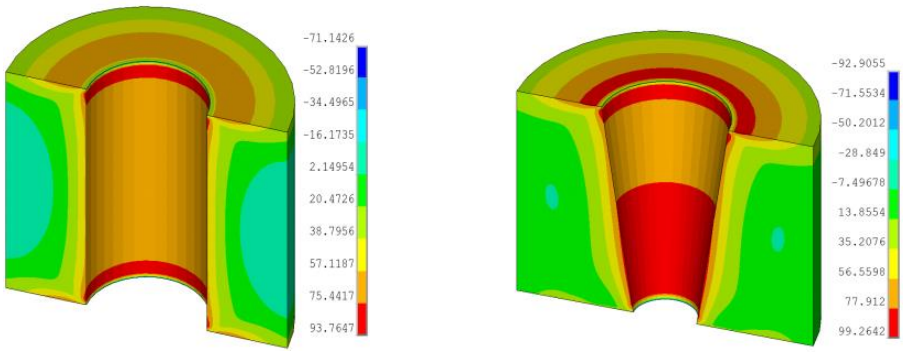
D_{exit}: TPV exit diameter

H_{glass}: Glass thickness

$H_{polymer}$: Polymer thickness

For a TPV with 60 µm entrance diameter in 100µm thick glass, electrical discharge process led to a tapered via profile with an exit diameter of 45 µm, corresponding to a taper angle about 4.3°. Stress distribution in tapered TPV and straight TPV is given in Figure 3.33 in a comparative manner. Higher stress is observed at the exit region with smaller diameter. This is an expected result because, for a constant copper thickness, as diameter decreases, the structure

approaches that of a fully copper-filled via. However, taper does not create significant difference in stress distribution. Therefore, for parametric studies, quarter TPV model can be used.



(a) **(b)**

Figure 3.33. Distribution of 1st Principal stress, MPa, in glass for 60µm (a) TPV with no taper, (b) TPV with taper

Change of maximum first principal stress in glass with taper angle is shown in Figure 3.34 where the exit diameter of the TPV is reduced from 60 µm to 20 µm gradually. First principal stress in glass increases with TPV taper due to decreasing exit diameter. Therefore, from reliability standpoint, via formation methods should be optimized for lower TPV taper.

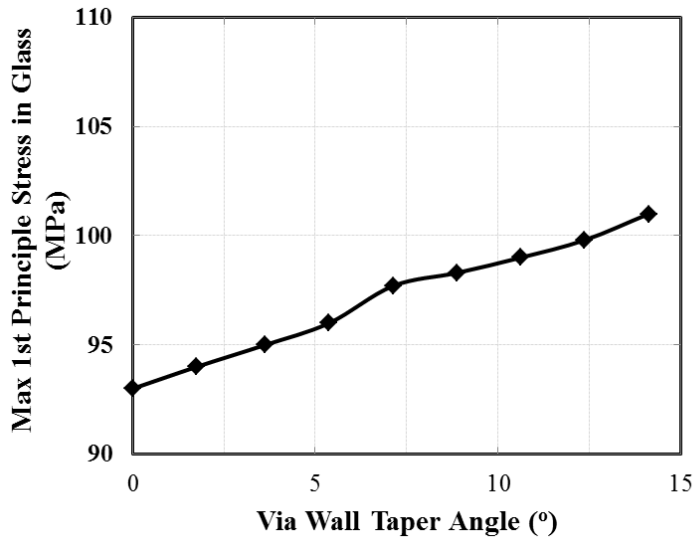
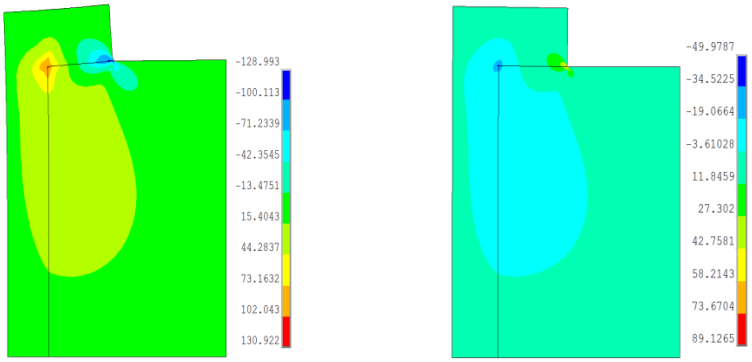


Figure 3.34. Effect of TPV taper on first principal stress in glass

3.4.1. Effect of Polymer films on glass:

The purpose of polymer lamination is three folds: 1) improve glass-handling by minimizing impact on glass, 2) higher adhesion of copper to polymer compared to glass surface, 3). fill the defects on glass surface for easier glass handling.

Distribution of shear stress without polymer at both cold and hot thermal extremes is shown in Figure 3.35. High shear stress concentration is observed around the via pad, which can drive delamination of copper from the smooth glass surface, as observed previously. Polymer layer reduces the shear stress around the via pad and facilitates higher adhesion surface to copper, and thus mitigates the risk of copper delamination.



(a) **(b)**

Figure 3.35. Contour plots of shear stress, MPa (a) at -55°C, and at 125°C

Parametric studies are performed with different thicknesses of polymer, while keeping other parameters constant. This analysis can provide guidelines for selecting the optimum polymer thickness. Variation of maximum 1st principal stress in glass with polymer thickness is illustrated in Figure 3.36. The maximum first principal stress in glass at cold extreme does not significantly change with the existence of a thin polymer. Beyond 5 µm thickness, polymer does not significantly alter the stress magnitudes up to 15 µm. The maximum stress decreases by about 15% as the thickness of polymer liner decreases from 15 to 30 µm.

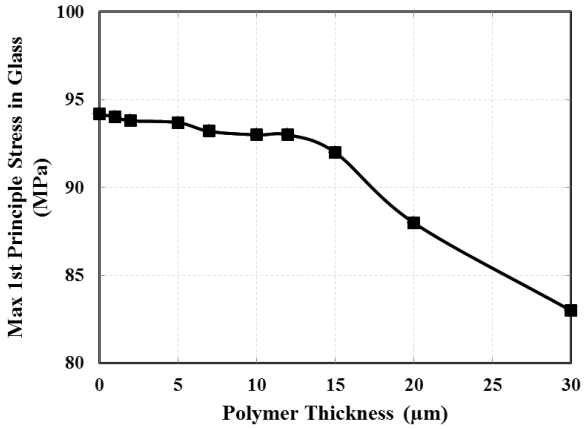


Figure 3.36. Variation of maximum 1st principal stress in glass, MPa, with thickness of polymer (µm)

3.4.2. Fatigue Life Prediction:

For a TPV of 60 µm diameter on 100 µm thick glass with 5 µm polymer and 10 µm of plated copper, total strain range is approximately 0.0039, corresponding to a fatigue life of above 7896 thermal cycles, as obtained from Equation 3.19. The results indicate that fatigue failure of copper is unlikely for TPVs in this study.

3.4.3. Impact of Curvature on Entrance and Exit

Electrical discaharge TPV formation leads to curvature on corners of via where high first principal stresses in glass are expected. This curvature reduces the stress in glass, thus leading to more reliable TPVs. As shown in Figure 3.37, a fillet radius of 3 µm in the corner led to approximately 20% reduction in first principal stress in glass along the sidewall and around TPV corner. As TPVs fabricated in this study have a curvature around entrance, first principal stress in glass is reduced, thus the chance of glass cracking is lowered.

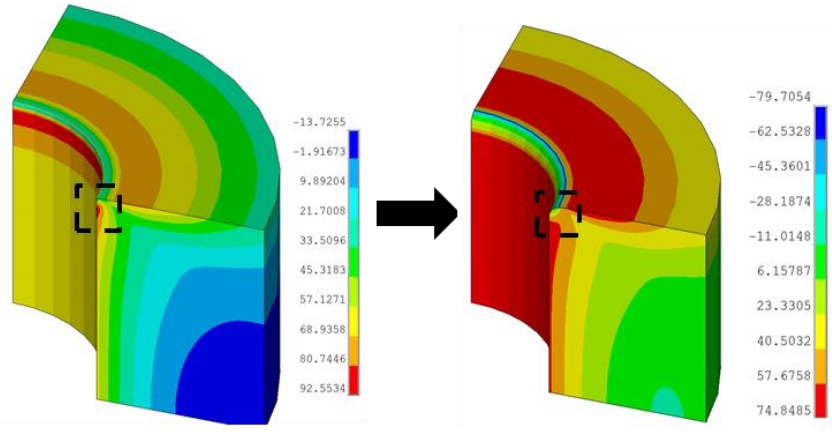
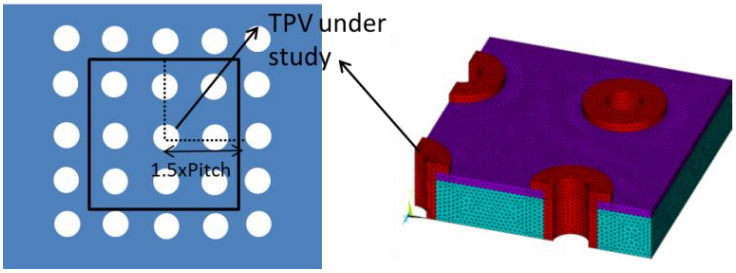


Figure 3.37.Contour plots of 1st principal stress in glass, MPa, at 125°C Stress reduction in via corner due to curvature

3.4.4. Impact of Neighboring TPVs

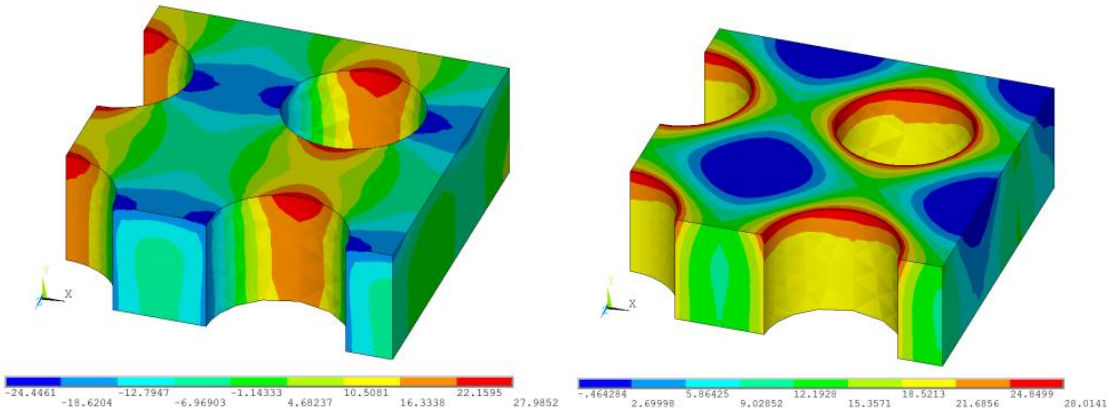
To capture the impact of neighboring TPVs, 3D TPV models are built according to the unit cell shown in Figure 3.38. A quarter-symmetric structure with appropriate boundary conditions is modeled. Symmetric boundary conditions are applied to the inner surfaces, and periodic boundary conditions are applied to the outer surfaces.



(a) **(b)**

Figure 3.38. Finite element analysis for evaluating the impact of TPV pitch: (a) Unit cell used for modeling and (b) meshed model of 1/8th TPV with neighboring vias

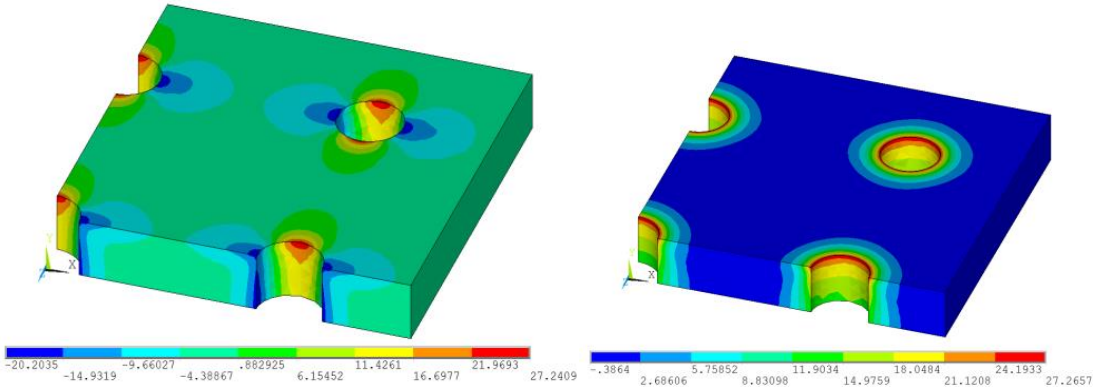
The contour plot of 1st principal stress in glass at 125 ^{o}C is shown in Figure 3.39 for TPVs at 100 µm pitch. It is observed that, due to the elastic interaction between TPVs, stresses in Cartesian x direction (σ_{xx}) are intensified in the regions that are closest to the adjacent TPVs. On the other hand, 1st principal stress is symmetrically localized around the vicinity of TPVs and stresses between TPVs are much smaller.



(a) **(b)**

Figure 3.39. (a) Contour plots of (a) stress in Cartesian x direction, σ_{xx}, MPa (b) 1st principal stress, MPa in glass for 100 µm pitch

The corresponding stress distribution when the TPV pitch is increased to 220 µm is shown in Figure 3.40. The elastic interaction between TPVs is reduced; however, 1st principal stresses in glass reduces by only ~2.7%.



(a) **(b)**

Figure 3.40. (a) Contour plots of (a) stress in Cartesian x direction, σ_{xx}, MPa (b) 1st principal stress, MPa in glass for 220 µm pitch

The impact of neighboring TPVs on maximum 1st principal stress in glass is not significant above 1.5x diameter for annular TPVs with 10 µm copper thickness. For TPVs fabricated in this study, via pitch is 220 µm, approximately four times the 60 µm via diameter. Therefore, the impact of neighboring TPVs is negligible. Furthermore, as discussed earlier, fabrication processes are double-sided, which eliminates the potential for warpage that can impose a strain distribution on the panel. Probability of failure can be assumed identical for all TPVs, independent of the location in the glass panel.

3.5. TPVs after IC Assembly

This section focuses on modeling of TPVs in 3D glass packages to assess the effect of parameters such as glass CTE, and other material properties and via geometry on reliability of TPVs under thermomechanical loading. Ansys^{TM} finite element modeling software with temperature-dependent properties of materials was used for modeling the glass TPV test vehicles. These materials are glass, polymers dielectric films that are laminated onto the glass substrate, solder resist, silicon die and lead-free solder bumps. Material properties of these are summarized in Table 5 and temperature-dependent properties of solder are compiled in Table 6. Bi-linear kinematic hardening model with 172MPa yield stress and 1034 MPa modulus is used for copper in order to capture the plastic deformations. Geometric properties for modeling are summarized in Table 7.

Table 3.5 Material Properties Used in mechanical modeling

	Elastic Modulus (GPa)	Poisson's Ratio	CTE(ppm/^{o}C)
Glass	77	0.22	3.8
Polymer	6.9	0.3	31

Copper	121	0.3	17.3
Underfill	10.5	.261	75
Silicon	130	.28	2.7
Solder	Temp-dependent	.4	22

Table 3.6 Temperature- Dependent Properties of Solders

Temperature (K)	233	263	293	333	373
Modulus (GPa)	31.8	27	20.1	16	12.1
Yield Stress (MPa)	35	30	25	16	12
Tangent Modulus (MPa)	116.7	116.7	66.7	25	16.7

Table 3.7 Geometric Properties

Glass Thickness (µm)	100
Glass width and length (mm)	12
Polymer thickness (µm)	20
Solder Resist thickness (µm)	10
Solder bump width/height (µm)	100
Solder bump pitch	100
TPV Diameter / pitch (µm)	60 / 200
Die Thickness (mm)	0.6
Die width / length (mm)	5/5

For enabling double-side assembly processes, warpage should be controlled after the first assembly on one side, in order to enable assembly of the second die on the other side. It is, therefore, important to predict warpage of the glass interposers after assembly. Finite element models in 2D were created and simulated using the material and geometric properties. The simulation starts with heating the system up to underfill cure temperature, followed by cool-down to -55°C. Simulation results, as illustrated in Figure 3.41, show that the maximum warpage of glass interposer is around the edge and it is approximately 0.02mm for a 12mm square glass interposer.

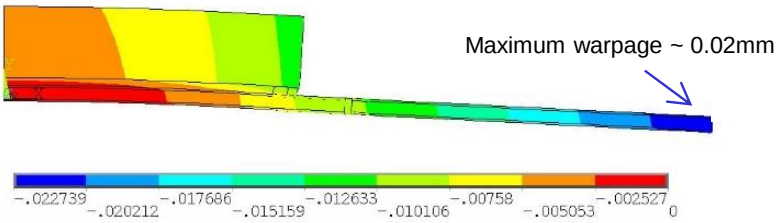


Figure 3.41. Scaled view of glass warpage after assembly (mm)

Reliability of vias in a free-standing glass interposer was investigated in the prior studies. From the simulations, it was observed that the material junctions and interfaces are the critical regions for failure during thermal cycling. The plastic strains in copper were low, indicating high fatigue life. Moreover, laser drilling of glass results in ultra-small surface defects that do not lead to cracking of glass under thermal load. In order to study the stress around TPV in package; cut-boundary method was used based on Saint Venant's principle [84]. Local TPV model was simulated using boundary conditions from a global model. Two-dimensional models of the free-standing glass interposer with TPV and package with an assembled die are shown in Figure 3.42.

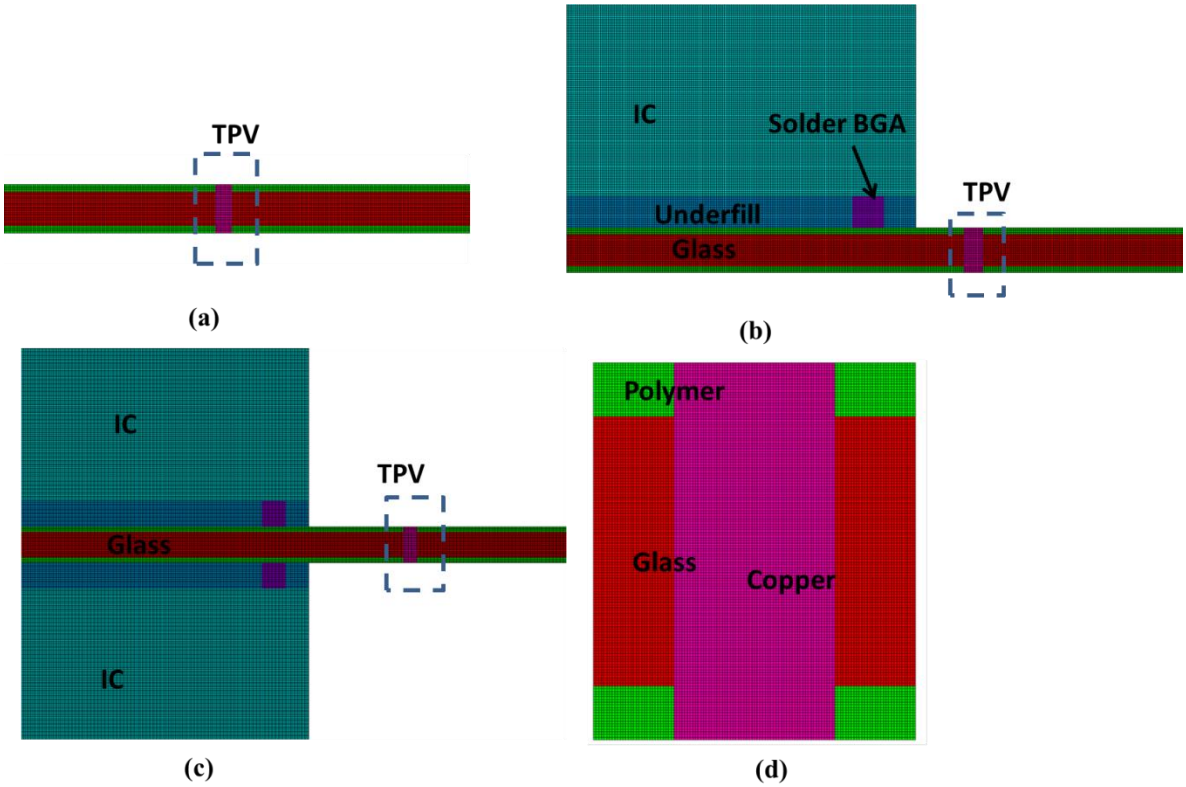


Figure 3.42. (a) Global model of tpv in free-standing glass interposer (b) global model of TPV with IC on one side, (c) double-side assembly and (d) local model of TPV with denser mesh and boundary conditions imported from global model.

A sample simulation result that illustrates the shear stress distribution of the global model is shown in Figure. 3.43.

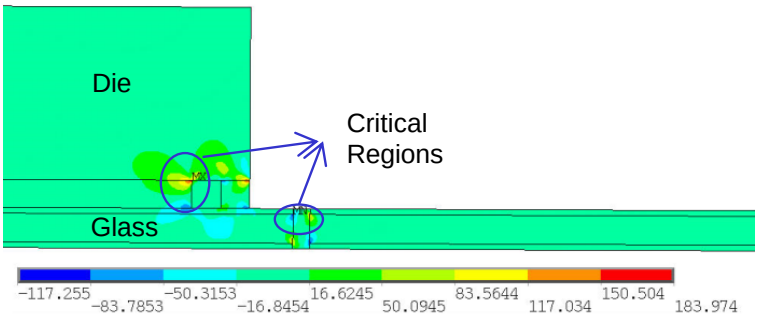
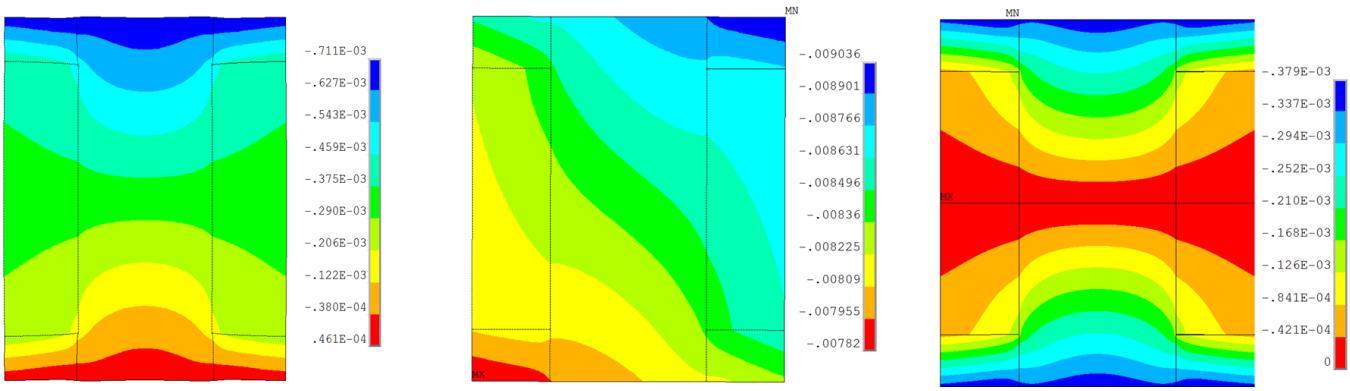


Figure. 3.43. Global model showing shear stress distribution after cooling (MPa).

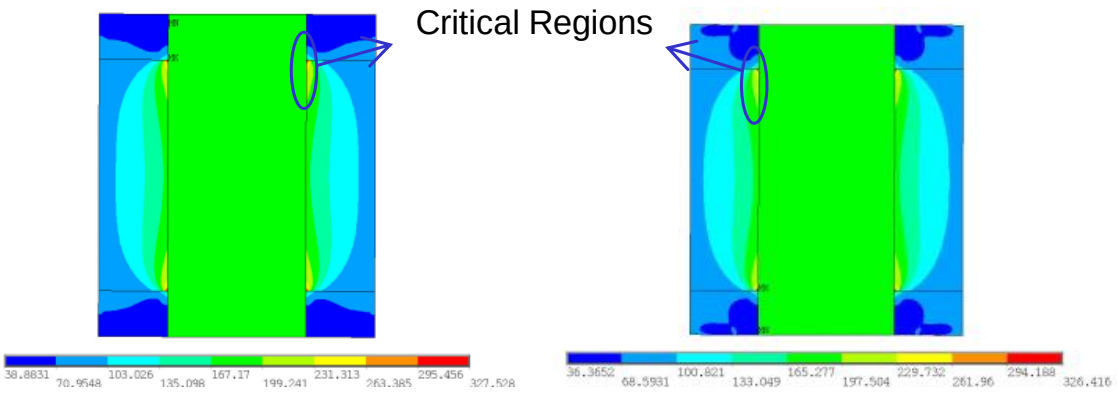
Figure 3.44 shows the out-of-plane displacements for TPVs in free-standing glass, and TPVs with die assembly. For TPVs in free-standing interposers, displacements are dominated by thermomechanical deformation, whereas TPV deformation in assembled packages is mainly due to warpage. In both free-standing and double-side assembly glass interposers, warpage is zero, so deformation in TPV is purely due to stress from CTE-mismatch.



(a) **(b)** **(c)**

Figure 3.44. Out-of-plane (u_y, mm) displacement in (a) (left) free-standing TPV, (b) (right) TPV with single side IC assembly and (c) with double-side assembly

Local model of TPVs in a free-standing glass package is shown in Figure 3.45, illustrating the von Mises stress distribution around TPV with more resolution. It was observed that the material junctions are critical regions for failure in both cases and stress distributions and magnitudes are similar.



(a) **(b)**

Figure 3.45. Local TPV model showing Von Mises stress (MPa) distribution after cooling (a) package (b) free-standing glass interposer.

Figure 3.46 illustrates the distribution of radial stress in TPV at -55^{o}C in a free-standing glass interposer, with die on one side and with dies on both sides. As seen, the distribution and magnitude of radial stress is approximately identical for all scenarios. This shows that, IC assembly does not have a big impact on the reliability of TPVs. If solder bump is not directly on TPV, impact of single or double-side assembly on TPV stress is negligible. On the other hand, if solder bump is directly placed on TPV pad, radial stress on surrounding glass becomes compressive which reduces the probability of copper delamination along TPV sidewall.

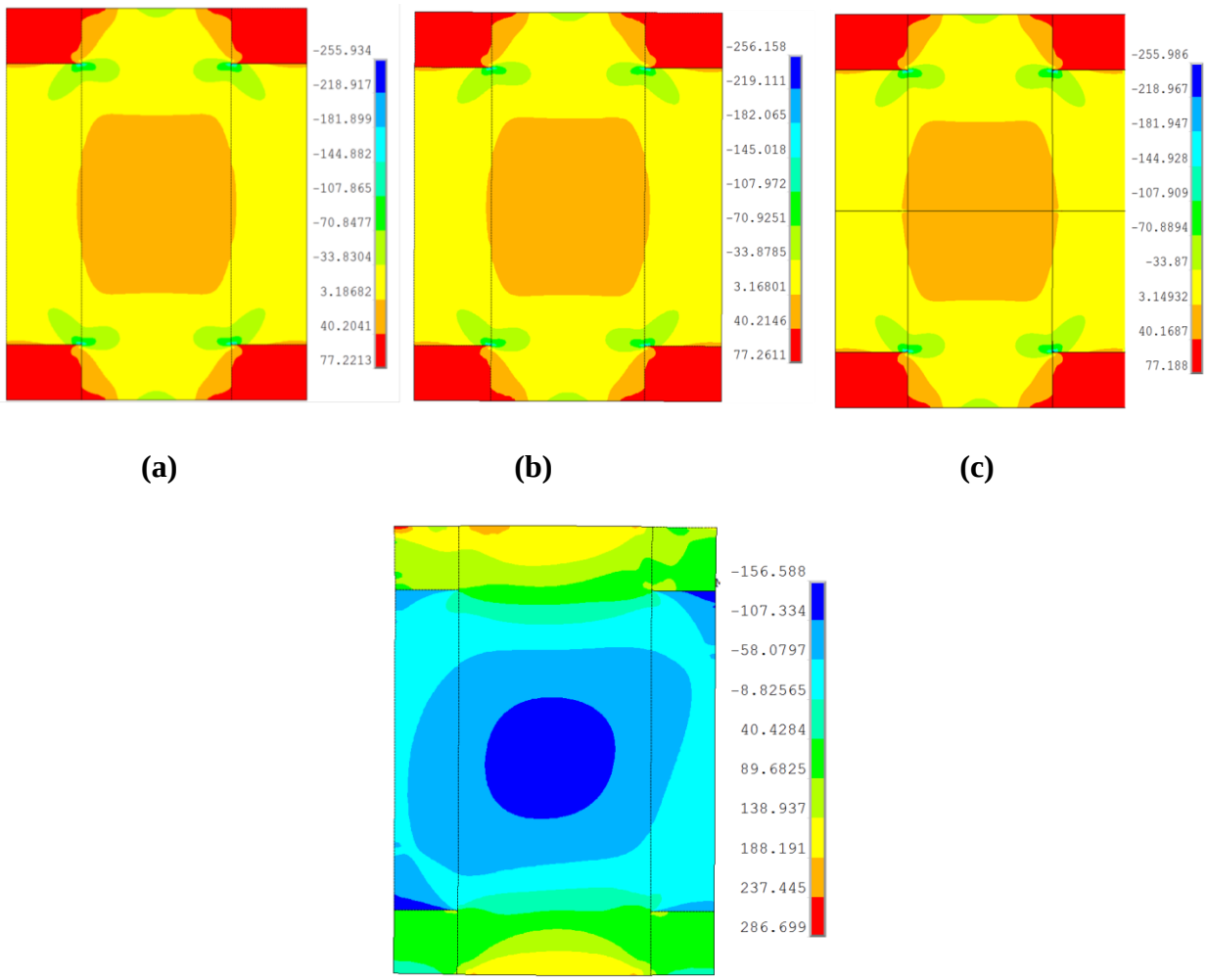


Figure 3.46. Local TPV model showing radial stress (MPa) distribution at -55^{o}C in (a) free-standing glass interposer, (b) glass interposer with single side assembly, (c) double-side assembly and (d) solder bump is directly on TPV with single side assembly

For high-bandwidth applications, short distances between solder bump to TPV are preferred to reduce the time for signal propagation. In order to assess the effect of this distance, the via stresses were modeled when this parameter is systematically decreased from 500µm to 0µm (0µm refers to via-on-pad structure). Von Mises stress around via is considered as the design parameter. Figure 3.47 shows the change of stress with distance. The stress increases by

15-20% as the distance between bump and TPV reduces from 50 μm to 0 μm (or via-on-pad structure). Placing the solder bump directly on TPV leads to higher von Mises stress around TPV.

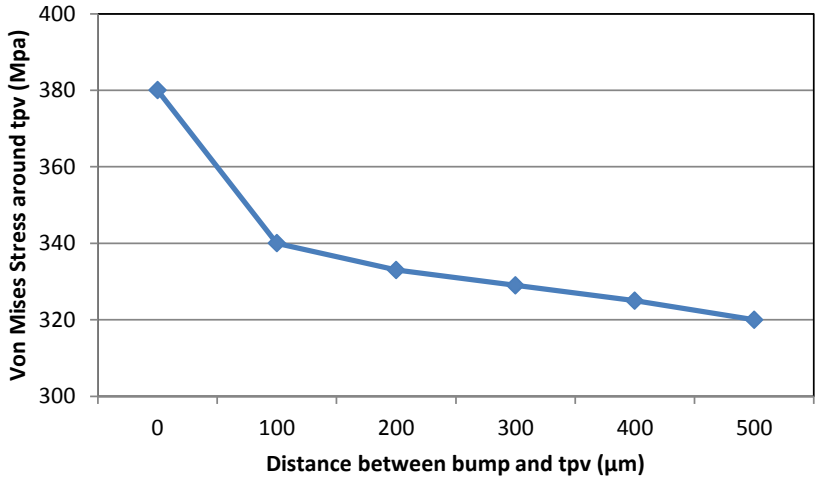


Figure 3.47. Effect of bump-TPV distance on via stress.

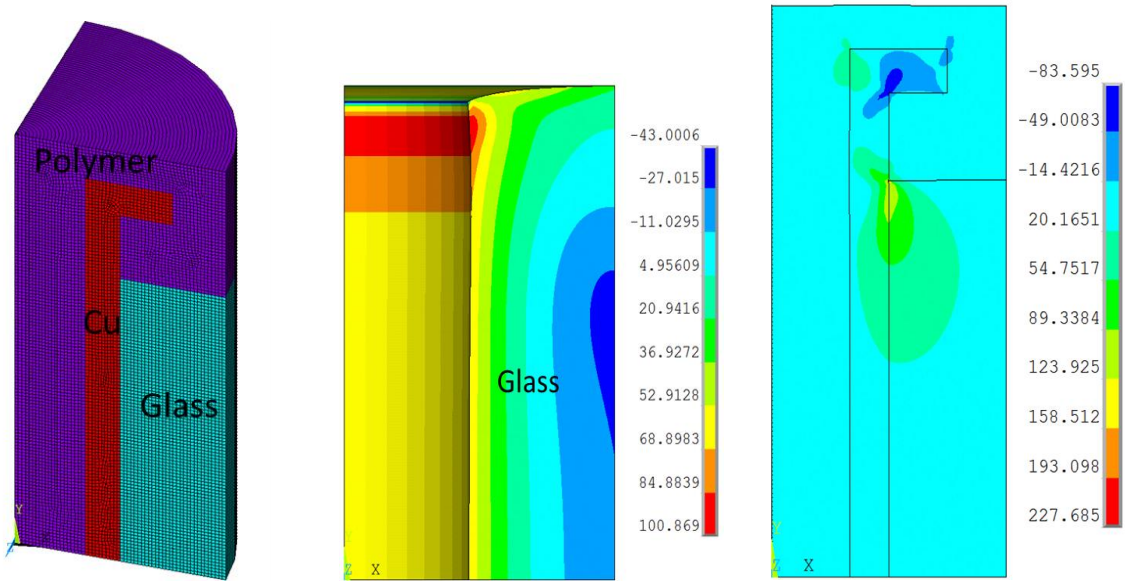
These simulation results show that IC assembly and related warpage do not significantly alter the stress distribution in TPVs. The distance between solder bump and via does not have significant impact unless it is a via-on-pad type structure. Based on these results, TPV in glass interposer with component assembly is estimated to be as reliable as TPV in free-standing glass. In thermal cycling test, failures are expected to occur first in solder bumps instead of TPVs.

3.6. TPVs with polymer lining or polymer filling

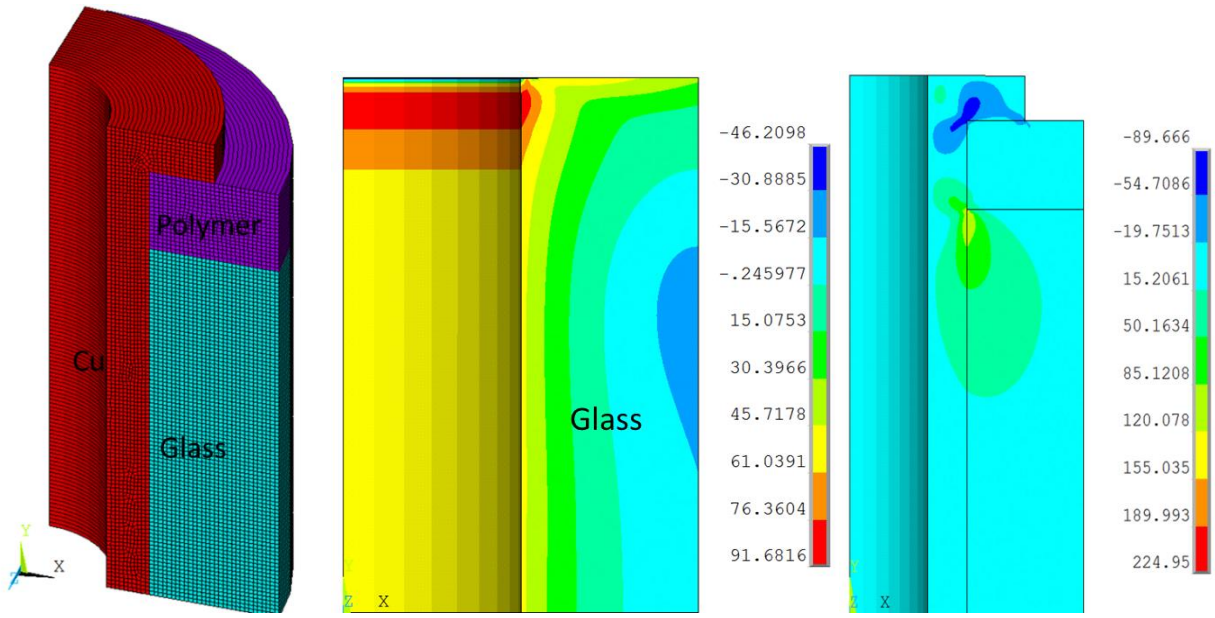
This section explores thermomechanical stresses in different TPV configurations: 1) Filling of vias with polymer, subsequent to metallization and 2) fabricating a polymer liner along the via sidewall prior to metallization.

3.6.1. Polymer-filled TPV

Annular plating of TPVs reduces the thermomechanical stress on via walls. However, in some applications, a second polymer is laminated on both sides in order to create a multi-layer structure. In these cases, the second polymer might flow and fill the hollow region inside the TPVs. Furthermore, in order to land a die directly on via, annular TPV needs to be filled. Therefore, there is a need to study the impact of polymer filling of TPV.



(a) **(b)** **(c)**



(d) **(e)** **(f)**

Figure 3.48. (a) Meshed model of polymer-filled TPV, (b) 1st principal stress (MPa) (c) Shear stress (MPa) at -55°C (d) meshed model of annular TPV, (e) 1st principal stress (MPa) (f) Shear stress (MPa) at -55°C

Figure 3.48 illustrates the distribution of thermomechanical stresses in polymer-filled TPV in comparison with annular TPV. It is observed that polymer filling of the hollow region inside TPV does not reduce the thermal stresses in glass. Instead, it leads to slightly higher stresses.

3.6.2 TPVs with Polymer Liner

Laminating the sidewall of TPVs with polymer reduces the thermomechanical stress in glass by eliminating the contact between copper and glass. Figure 3.49 shows the meshed model

and corresponding thermomechanical stresses for a TPV with polymer liner.

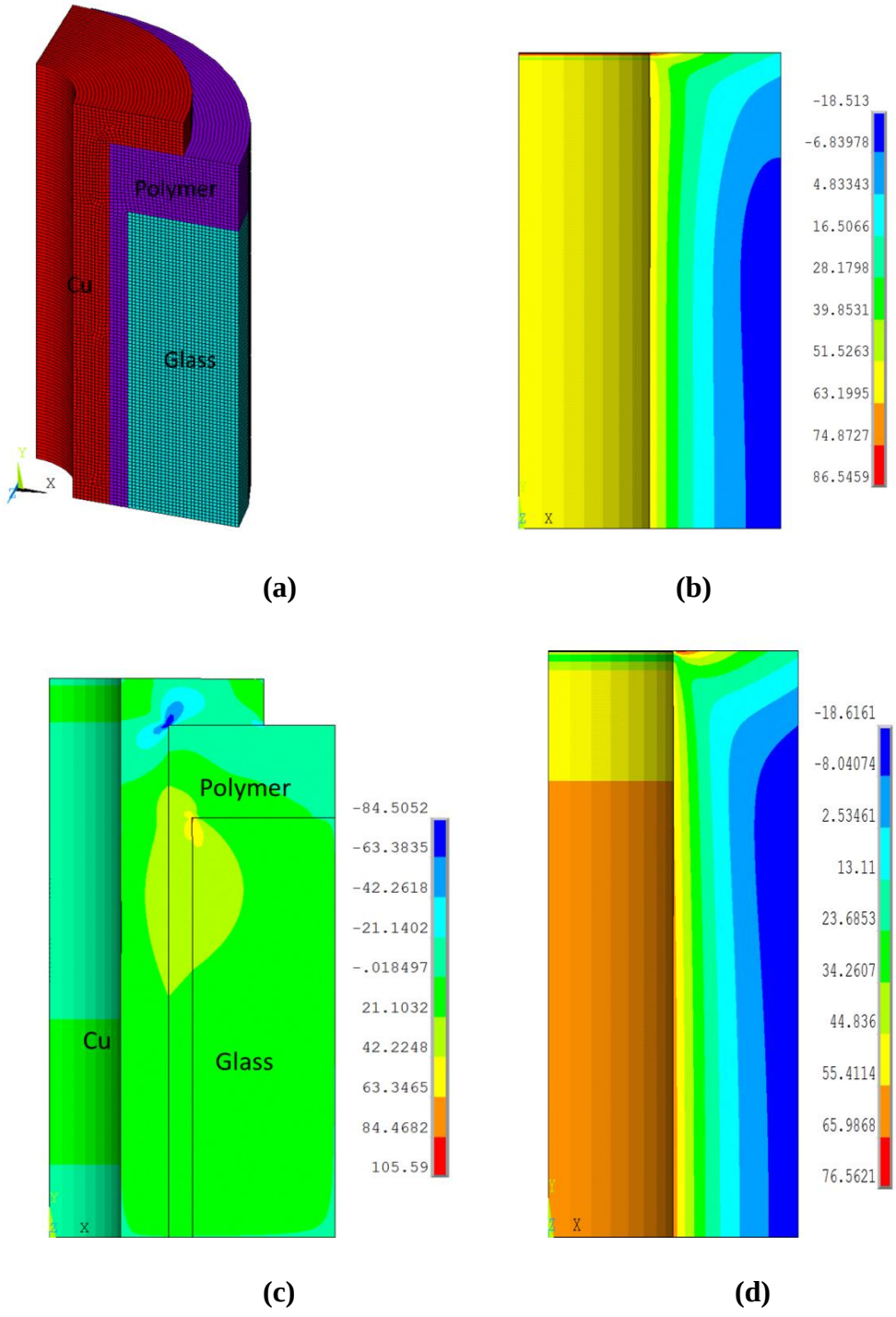


Figure 3.49. (a) Meshed model of TPV with sidewall liner, (b) first principal stress (MPa) in glass, (c) shear stress (MPa) in TPV, and (d) radial stress(MPa) in glass at -55^{o}C.

Polymer liner helps alleviate thermomechanical stresses. This effect can enhance the reliability of TPVs with thick copper, required in high-power applications for current-carrying or as thermal vias for heat spreading. Figure 3.50 shows the variation of first principal stresses along the via sidewall. As observed, even a 5 µm thick polymer liner reduces the stress significantly. However, additional increase in liner thickness does not change the stress dramatically.

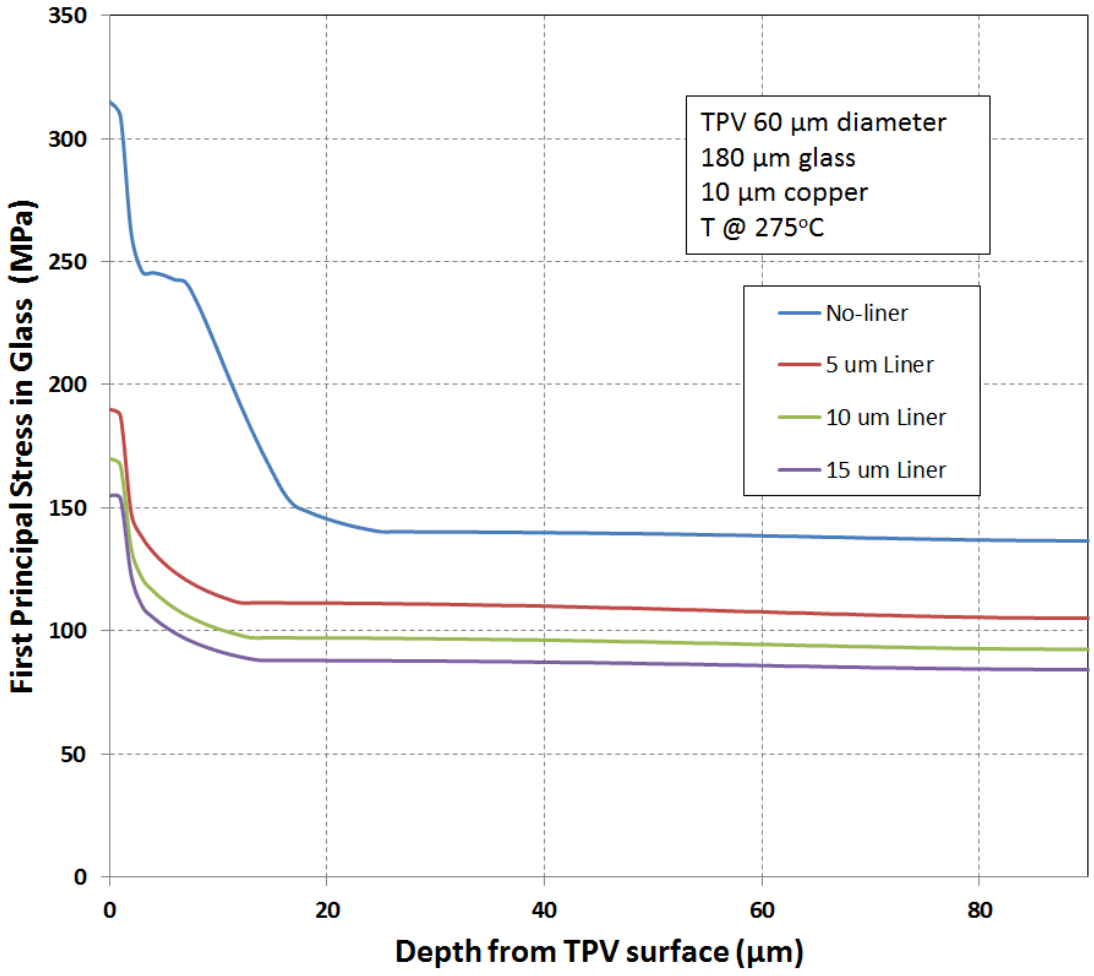
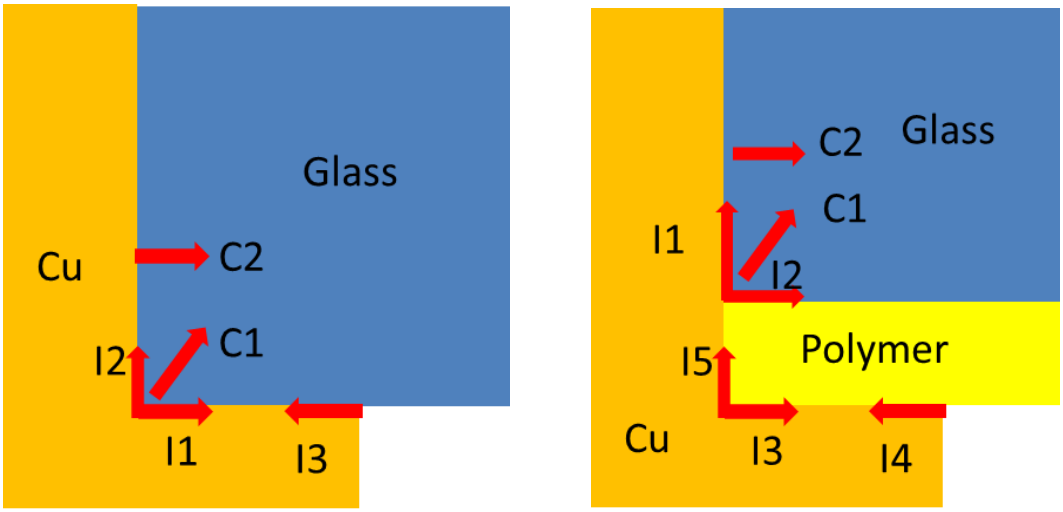


Figure 3.50. Variation of principal stress in glass with varying liner thicknesses

3.7. Fracture Mechanics Analysis of delamination and glass cracking

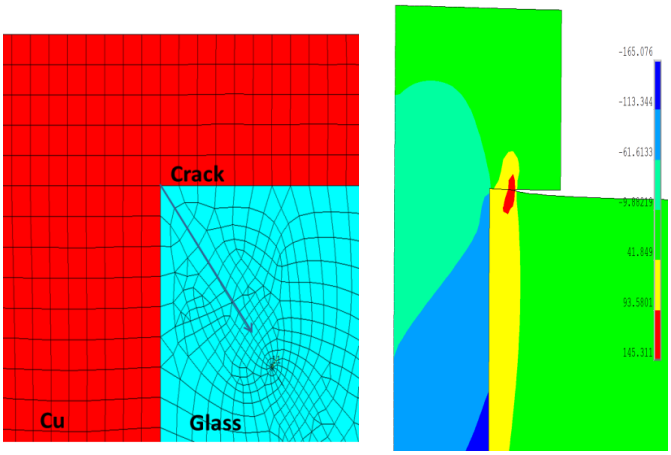
The stress and strain analysis provides a general view of possible critical locations. In this section, fracture analysis is carried out by building interfacial (I) and cohesive (C) cracks into two TPV models – bare glass and polymer-laminated glass . For cohesive fracture in glass, cracks were assumed to grow along 45^{o} location and horizontal as depicted in Figure 3.51[85].



(a) **(b)**

Figure 3.51. Cracks built into TPV into (a) bare glass and (b) polymer-laminated glass

TPV with a diameter of 30 µm in 100 µm glass was modelled with 10 µm conformal copper plating. A crack length of 5 µm was used for both cracks. TPV models were heated to a temperature of 125 ^{o}C and also cooled to a temperature of -55^{o}C. Energy release rates corresponding to each defect were calculated using J-integral method. Figure 3.52 illustrates the mesh used for glass corner crack and axial stress for interfacial crack in copper pad. Crack formation in copper or polymer is unlikely because they are both ductile materials with high critical strain energy release rate (G_c). Therefore, cohesive failure in glass is of concern along with interfacial failures in copper/glass, copper/polymer and polymer/glass interfaces. The results are summarized in Table 8 and Table 9.



(a) **(b)**

Figure 3.52. (a) Meshed model for corner crack and (b) axial stress for copper pad delamination from the right side.

Table 5.8 G values of cohesive and interfacial cracks in TPV in bare glass

		125°C		-55°C	
		G(J/m^2)	Open/Close crack	G(J/m^2)	Open/Close crack
Interfacial	I1	0.00752	Open	0.00032	Close
	I2	0.2791	Close	2.923	Open
	I3	0.1536	Close	0.1946	Open
Cohesive	C1	0.02341	Close	0.1813	Open
	C2	0.2234	Open	0.1285	Close

Table 5.9 G values of cohesive and interfacial cracks in TPV in polymer-laminated glass

		125°C		-55°C	
		G(J/m^2)	Open/Close crack	G(J/m^2)	Open/Close crack
Interfacial	I1	0.3167	Open	2.8547	Close
	I2	0.1525	Close	0.1237	Open
	I3	0.00781	Close	0.0061	Open
	I4	0.02428	Close	0.17431	Open
	I5	0.01784	Close	0.1687	Open
Cohesive	C1	0.02182	Close	0.1731	Open
	C2	0.2196	Open	0.1115	Close

The experimentally-determined critical G_c values (~20 J/m^2 for polymer/glass delamination failure, ~5 J/m^2 for copper/polymer delamination failure and 8.9 J/m^2 for cohesive crack growth) are much higher than the values reported in Table 8 or 9. Based on these results, it is seen that copper delamination in the via pad is more likely to initiate from copper pad edge [86]. Polymer layer creates a high adhesion surface, thus reducing the probability of the via pad delamination. Copper delamination along glass sidewall is of concern. The roughness in the glass via wall enables high bonding energy of copper/glass interface. Glass cracking at corner is more likely at cold temperatures; however, energy release rates for cohesive fracture are low, which means cracks would be arrested in glass. Energy release rate for debonding of polymer/glass interface is lower than critical energy release rate of the interface, which means that small delamination formed during laser drilling would not grow as predicted by FEM.

3.8. Summary and Overall Design Guidelines for TPVs

Thermomechanical stresses arising from CTE mismatch between materials in through-package-vias were explored with both analytical equations and finite element models. Analytical equations provided qualitative trends for reliable design of TPVs. Axisymmetric 2D and 3D models were developed in ANSYS to simulate the stresses in TPV under thermal cycling for both polymer-laminated and bare glass with via-first and via-last approaches. Through-package-vias in an assembled package was also simulated to investigate the impact of dies on reliability of TPVs. Impact of polymer-filling of hollow TPVs and polymer liner along sidewall was also investigated. Fracture models in 2D were built to estimate the energy release rates of possible failure modes.

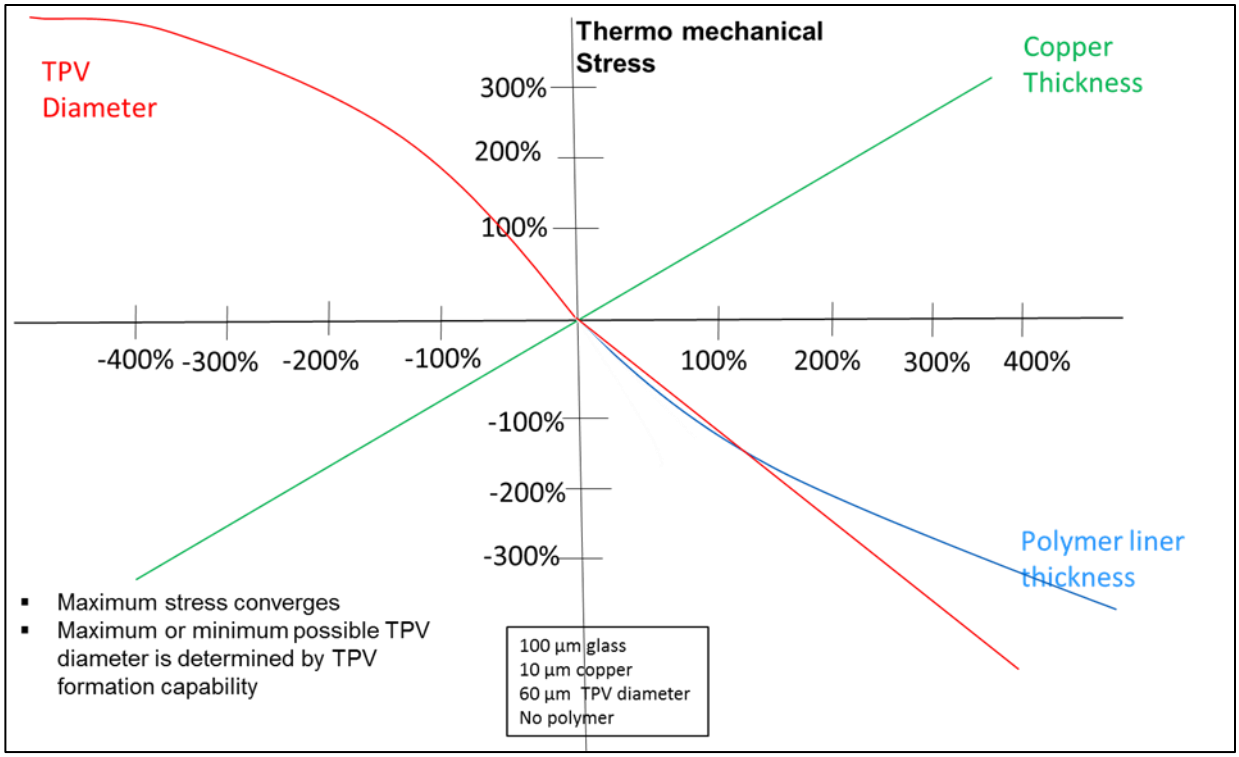


Figure 3.53. Sensitivity analysis of TPV parameters polymer thickness, diameter and copper thickness

The impact of geometric parameters on thermomechanical stress is illustrated in Figure 3.53 starting from a TPV with 60 µm diameter in 100 µm bare glass with a conformal plated copper of 10 µm. It is observed that increasing the copper thickness incrementally up to fully filling of via hole increases the stress in an approximately linear fashion as expected. Increasing the polymer thickness on glass surface reduces the stress on glass by increasing the distance between glass and TPV free-end. On the other hand, reducing the TPV diameter increases the stress by both increasing the aspect ratio (glass thickness/ TPV diameter) and diameter ratio ($\gamma = \frac{D_i}{D_{Cu}}$). However, with further reducing the TPV diameter the impact of aspect ratio tapers off as expected from modelling and stress magnitudes approach to 2-D analytical solutions. Therefore, the thermal stresses exerted on glass during thermal cycling converge to a maximum value determined by CTE mismatch. On the other hand, increasing the TPV diameter with constant copper thickness reduces the stress on glass. Therefore, minimum or maximum possible TPV diameters are determined by TPV formation quality which determines the size of defects. Figure 3.54 illustrates the distribution of 1st principal stress on glass at -55^{o}C for a fully-filled TPV with 10 µm diameter in 100 µm glass laminated with 20 µm polymer on both sides. High aspect ratio of 10 leads to a uniform stress distribution along the TPV sidewall which is converging to approximately a stress magnitude of 102 MPa due to CTE mismatch.

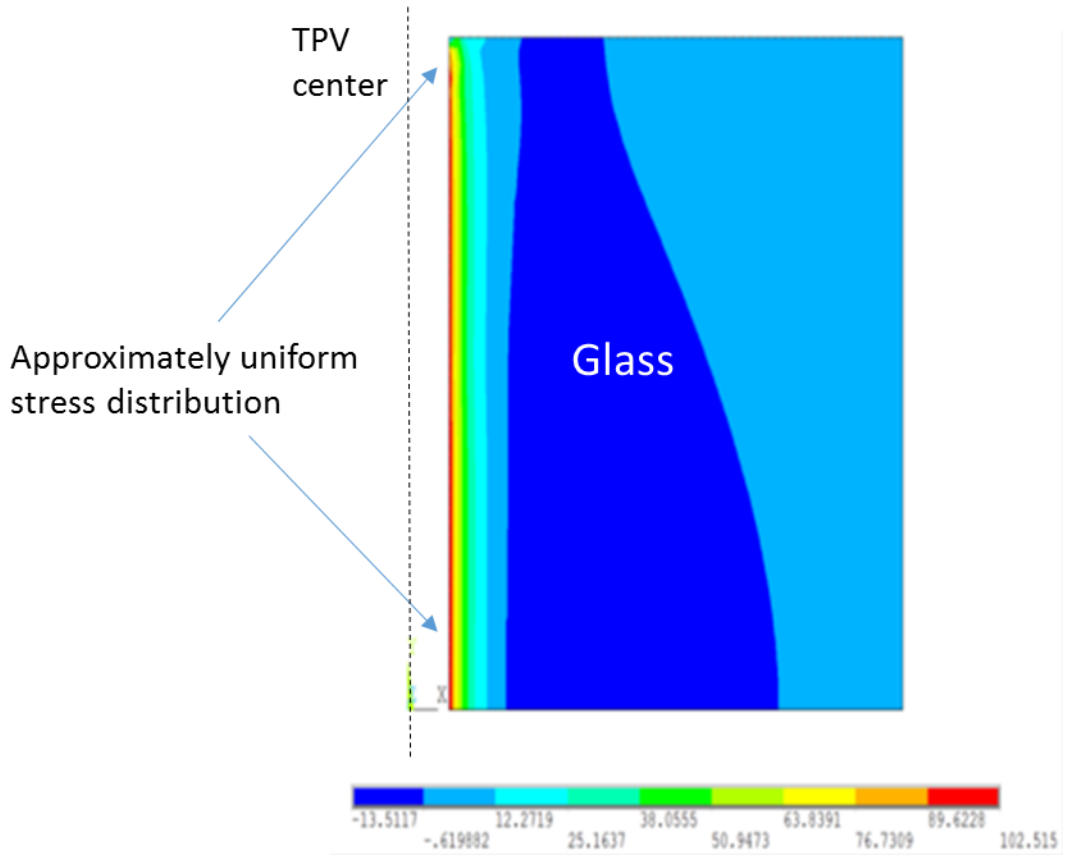


Figure 3.54. Distribution of 1st principal stress on glass at -55°C for an aspect ratio of 10.

Assuming the critical defect size given by $K_I = \sigma\sqrt{\pi a} \times 1.12$, critical defect size for brittle fracture can be estimated as 6 µm which is quite large. However, the geometry of defects can further increase the stress intensity factor which can become higher than fracture toughness of glass.

Based on these studies following design guidelines are suggested:

1) TPV diameter, copper thickness, and aspect ratio have the highest impact on glass stresses.

2) Reducing TPV diameter decreases the probability of glass cracking and copper delamination for TPVs with same aspect ratio. Thermomechanical reliability is of higher concern for fully - plated TPVs with diameters larger than 100µm. However, for conformal-plated TPVs, increase in diameter lowers the thermomechanical stresses in glass.

3) Thicker polymer lamination on surface leads to reduced stresses in glass by acting as a stress-buffer layer between copper and glass. Polymer films also improve processability by acting as an adhesion promoter for copper on glass surface.

4) For general package design rules, plastic deformation of copper is low and confined to a very small region around TPV corner. Therefore, fatigue failures in TPV are unlikely.

5) Impact of neighbor TPVs tend to fade away when the pitch exceeds twice the diameter. Pitch should be 2 x diameters to avoid stress interaction between TPVs.

6) Assembly of ICs on glass interposer does not significantly change stresses in TPV compared to free-standing glass, unless solder bump is directly placed on the via.

7) Glass cracking is the most likely cohesive failure to occur. However, for annular TPVs, the energy release rate for cohesive cracking in glass reduces as crack grows, which suppresses and eventually arrest the crack growth.

8) Copper/glass delamination is the most likely interfacial failure mode. The driving force for this failure mode increases with via diameter and copper thickness. However, roughness inside the via wall and polymer lamination on surface increases the bonding energy, and thus suppresses this failure mode.

9) TPV taper should be kept low for lower thermomechanical stresses.

10) Conformal plating reduces thermal stress on glass. If high copper thickness is required, TPV diameter should also be increased.

CHAPTER 4

MATERIALS AND PROCESSES FOR FABRICATION OF TEST VEHICLES

This chapter describes the processes for fabrication of various test vehicles for TPV reliability characterization. Test structures are fabricated on both polymer-laminated glass and bare glass using a variety of via-formation techniques, following different fabrication procedures. In addition, 3D glass interposer samples with TPVs and double side IC assembly were built to assess the impact of 3D assembly on TPV reliability. Therefore, this chapter is organized into four parts in that materials and fabrication processes for each of these different test vehicles are discussed. Section 1 describes the fabrication process of polymer-laminated glass interposers based on [7]. Section 2 describes the processes for fabrication of bare glass interposers. In Section 3, the via-first primer process is explained. Section 4 outlines the fabrication and assembly processes for fabrication of glass interposers with ICs assembled on both sides.

4.1. Fabrication Processes for Polymer-Laminated Glass Interposers

The process flow schematic for two-metal layer polymer-laminated glass interposers is illustrated in Figure 4.1. The low-cost and high-throughput fabrication process basically consists of two major steps: 1) TPV hole formation, and 2) TPV and surface metallization through a semi-additive process. Test samples were fabricated using 6” glass panels at 180 μm and 100 μm thicknesses. Fabrication consists of two main processes: TPV hole formation with laser ablation and simultaneous through-package-via and RDL metallization using a semi-additive approach.

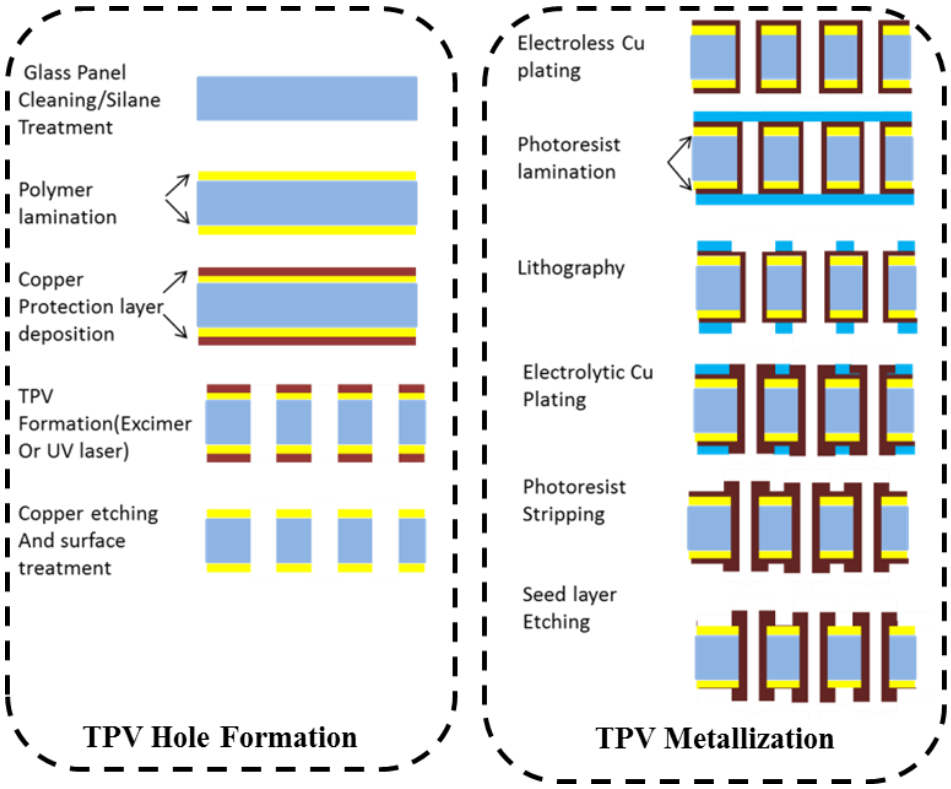


Figure 4.1. TPV fabrication process with (a) hole formation and (b) metallization.

4.1.1. TPV Hole Formation:

Fabrication process starts with cleaning of bare glass surfaces to remove organic residues using acetone, isopropyl alcohol (IPA) and deionized (DI) water respectively. It is followed by baking at 120^{o}C for 10 minutes to remove moisture. Subsequently, the bare glass surfaces were treated with silane coupling agents (3-Aminopropyltrimethoxy silane) to promote polymer to glass adhesion through the formation of -Si-O-Si bonds at the interface. In order to achieve low viscosity, silane was first diluted with methanol, and then applied on each glass surface followed by baking at 125^{o}C for 15 minute to dry and thermally attach silane onto glass. Silane films with a thickness of several nanometers were created on bare glass surfaces to enhance adhesion through the formation of chemical bonds. The nature of chemical bonds and modification of

glass surface chemistry after silane treatment is schematically shown in Figure 4.2. Covalent Si-O bonds are formed on the glass surface and the functional group (---NH_2) reacts with the polymer-chain molecules. Hence silane tends to bridge between glass and ZIF to improve the interfacial adhesion. The absence of silane coupling between polymer and glass were observed to cause adhesion failures resulting in polymer delamination during subsequent chemical processing steps.

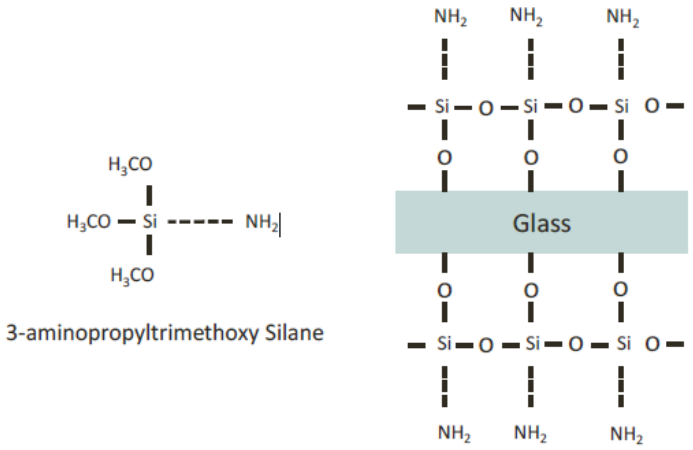


Figure 4.2. Silanization of glass for improved polymer-to-glass adhesion [87].

After silane treatment, the polymer was laminated on glass using a double-sided process to ease handling of glass during subsequent fabrication steps. The selection of polymer is based on following requirements: 1) Low electrical loss to achieve high performance, 2) Strong adhesion to glass to avoid delamination 3) Low modulus and CTE to improve reliability 4) high flow to fill defects on glass and via fill if necessary, 5) High glass transition temperature for high thermal stability, 6) High absorption of laser irradiation for efficient ablation, and 7) Smooth surface for fine line RDL formation. Based on these requirements, a cyclo-olefin resin system, named Zeon Insulation Film (ZIF) from Zeon Corporation Japan was selected due to its properties that are summarized in Table 4.1.1. In addition to its excellent dielectric properties

(loss tangent of 0.0011), ZIF material has low water absorption of 0.3%, which helps in achieving high insulation reliability between fine-pitch TPVs and RDL [88].

Table 4.1.Material properties of ZIF Polymer

Properties	Unit	ZIF
T_g (DMA)	^oC	162
CTE	ppm/ ^oC	31
Water Absorption (100^oC 1hr)	%	0.3
Elongation	%	3.6
Dielectric Constant (Dk)	(1~10 GHz)	3.1
Loss Tangent (Df)	(1~10 GHz)	0.011
Lamination Temperature	^oC	120
Young's Modulus	GPa	6.9
Laser Process-able	-	Yes
Flow-ability	-	Yes

Polymer lamination was carried out using a vacuum lamination tool in that both sides of the silicon substrate were laminated at the same time at 95℃. The stack-up used in the lamination chamber is shown in Figure 4.3. Thick Cu foils were used for protection and to avoid polymer contact with the lamination platens, which could have resulted in contamination and defects in the polymer surface. Such a double-side process can help to mitigate any potential

warpage of the thin glass panel generated by the heating and cooling cycles in the lamination process.

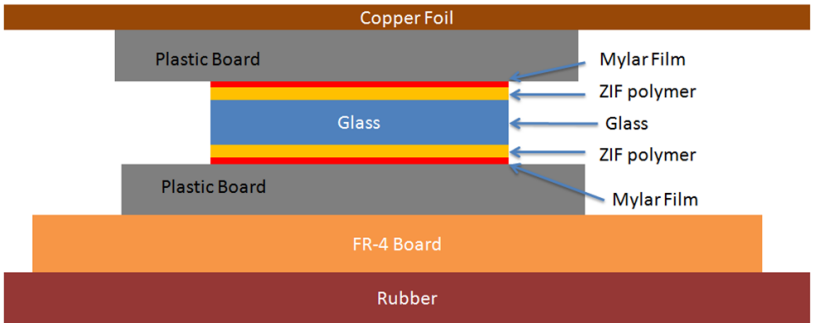


Figure 4.3. Schematic drawing of setup for vacuum lamination

After double-side lamination, a short hot press cycle was performed at 120℃ with 1 ton force for better planarity by eliminating any dimples resulting from the filling process. The schematic setup used for the hot press process is shown in Figure 4.4 and the stack was carefully designed to avoid any bending stress on glass to prevent any crack formation during the process.

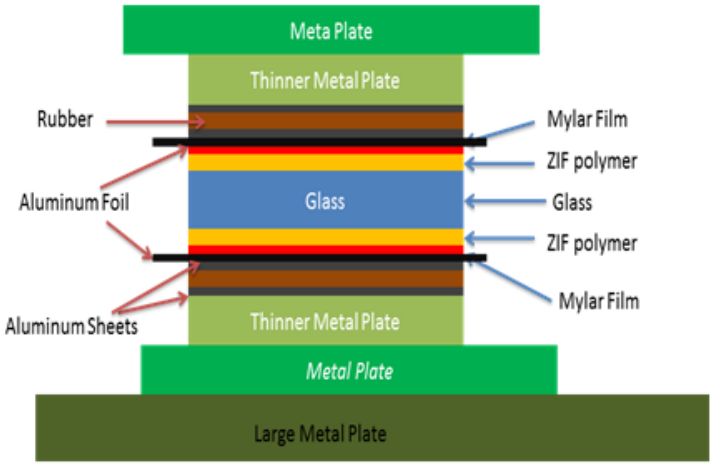
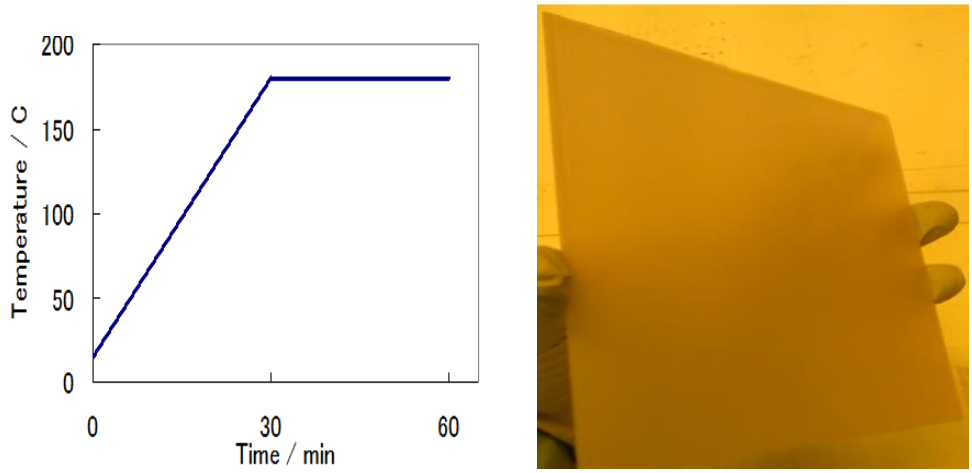


Figure 4.4. Schematic drawing of stack-up for hot press.

Thermal cure is required to complete the polymerization reactions at 180℃ for 30 minutes. The temperature profile for the ZIF curing is shown in Figure 4.5, along with an image of the polymer-laminated glass after curing. The mechanism can be explained as follows: Upon

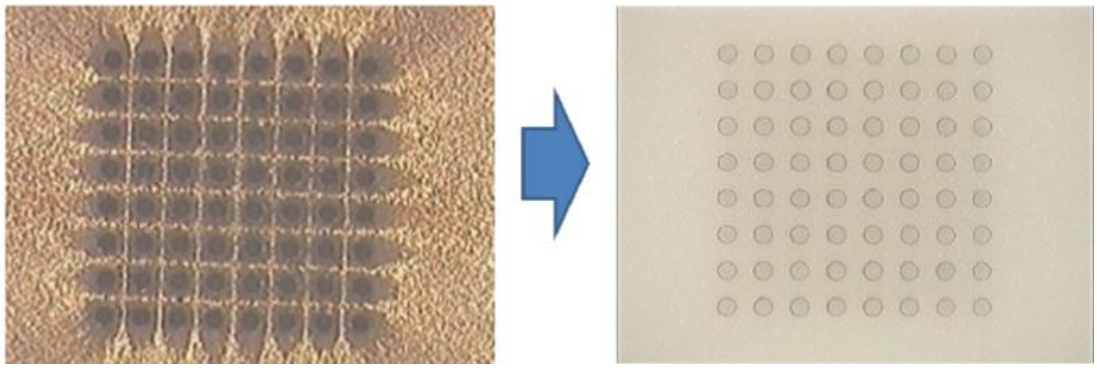
exposure to heat, the interaction of reactive oligomer groups occurs. This results in the increase of viscosity, cross-linking of polymer chains and thus hardening of the polymer.



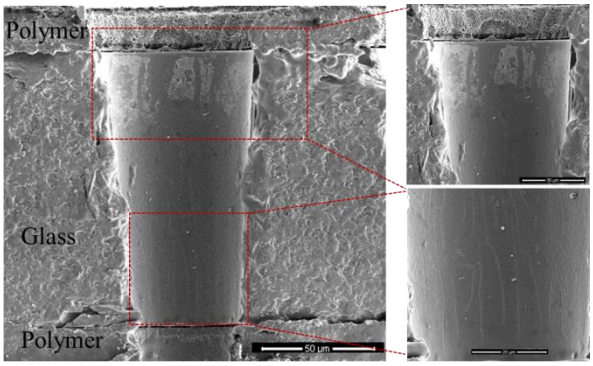
(a) **(b)**

Figure 4.5. (a) Thermal profile for ZIF polymer curing and (b) 6" polymer-laminated glass

After polymer lamination, a sacrificial copper layer is deposited on polymer-laminated glass surfaces to minimize debris on the polymer surface after ablation and to reduce thermal damage during via-formation by heat dissipation. A thin layer of copper (1μm) was deposited by electroless and electrolytic plating on the polymer surface prior to laser drilling. Laser drilling was used for TPV hole formation on polymer-laminated glass with copper protection layer. Three different types of lasers were utilized for via formation: ArF based 193nm excimer laser, 355 nm UV laser and CO_2 laser with 10.6 μm wavelength. Each via formation technique resulted in vias with different profile and defects. The copper was subsequently etched after via formation to remove residues off the surface as shown in Figure 4.6. Copper removal was achieved by $CuCl_2$ etchant.



(a) **(b)**



(c)

Figure 4.6. (a) TPV hole formation on copper + polymer laminated glass using ArF based excimer lasers (b) via array after copper removal, (c) SEM image of via cross-section

4.1.2. TPV Metallization

Metallization of the TPVs with thick copper film is required to complete electrical interconnections from top side to bottom side, and also for connecting components to each other and to the system board. The metallization process consists of two steps: 1) double-side electroless plating for Cu seed in TPVs, followed by patterning and 2) electrolytic Cu plating. This section summarizes the key steps and mechanisms for both processes.

Electroless plating forms a thin layer of copper seed (usually 100 nm-0.5 μm) on the polymer and glass via walls to provide electrical conductivity and allow the TPVs to be electrolytic-plated to final thickness thereafter. Unlike electroplating, electroless plating uses chemical reactions to deposit metal on the surface without any external electrical source. Prior to the electroless plating, a desmear process is necessary to treat the polymer surface. Such a step roughens the smooth surfaces of the polymer to improve adhesion between Cu and the polymer liner. For the ZIF polymer, the desmear process was divided into a few steps, as illustrated in Figure 4.7: Sweller (swelling of polymer), Permanganate ($KMnO_4$ to etch polymer surface to increase roughness) and Reducer (remove residue of permanganate). These steps are summarized in Table 4.2.

Figure 4.7. Detailed steps for desmear process

Table 4.2. Chemical Desmear for ZIF

#	Name/Process	Function
1	Sweller	Swelling resin to ease the removal of smear by permanganate bath
2	Rinse	DI Water
3	Permanganate	Oxidize smear to be removed and roughen the surface of polymer
4	Rinse	DI Water
5	Reducer	Reduce remaining permanganate on a surface
6	Rinse	DI Water

Cu electroless plating was performed by reducing complexed copper with formaldehyde in an alkaline solution. The reaction is catalyzed by palladium, deposited on the surface in a previous activation step. The Cu electroless plating process is governed by the reaction formula:

$$CuSO_4 + 2HCHO + 4\,NaOH \xrightarrow{Pd} Cu + 2HCO_2Na + H_2 + 2\,H_2O + Na_2SO_4$$

The Cu seed layer of thickness between 0.4 µm and 0.5 µm was deposited by electroless plating. The process steps are summarized in Figure 4.8. Conditioning and pre-dip steps clean the polymer surface by removing any residues and prepare the surfaces for the catalyst deposition. Palladium catalyst is formed on the surface and sidewall liners during the activation process and acted as activation sites for the subsequent electroless Cu. The last step, acid dip, was to clean the copper surfaces prior to electrolytic plating. The process sequence for electroless plating is illustrated in Table 4.3. Electroless plating is followed by annealing at 110^{o}C for 30 minutes to improve glass-copper adhesion and reducing residual stresses by recrystallization and grain growth. Peel strengths of greater than 0.7 kN/m have been demonstrated in prior work on copper metallization of ZIF polymer.

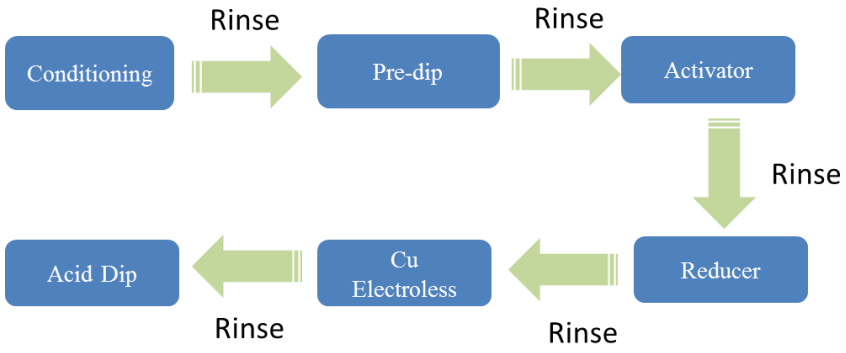


Figure 4.8. Detailed steps for electroless Cu plating

Table 4.3.Electroless copper plating process sequence

#	Name/Process	Function
7	Conditioner	Remove residues and soils from the surface and holes, conditions the glass and resin to ensure proper catalyst adsorption to these surfaces
8	Rinse	DI Water
9	Rinse	DI Water
10	Pre-dip	Protect copper contamination in the catalyst and provides common ion drag-in to the catalyst
11	Activator	Deposit palladium on the surface and wall of the hole. The palladium will then act as an activation site to initiate electroless copper deposition.
12	Rinse	DI Water
13	Reducer	Provides negative charges for reducing the copper ion to metallic copper
14	Rinse	DI Water
15	Electroless copper	Deposit a copper coating on the board surface and along the hole wall.
16	Rinse	DI Water
17	Acid Dip	Clean the copper surface
18	Rise	DI Water

After seed layer deposition, a dry film negative photoresist (PR) was laminated on both sides of the sample using a roll laminator. UV exposure through a mylar mask was carried out to photo-image the features that need to be copper-plated. Sodium Bicarbonate ($NaHCO_3$) was used as the developer solution. The minimum feature size that can be defined depends on the PR material properties, masks and processing conditions (exposure dose, development chemistry and speed). The TPVs and RDL layers on either side of the core were simultaneously electroplated. The plating current can be adjusted to vary the copper deposition rate. Prior to proceeding with electrolytic plating, plasma ashing was applied with CF_4-O_2 chemistry at 100^{o}C and 400 Watts RF power for 5 minutes on both sides to remove any remaining photoresist residues.

Cu electrolytic plating is the most widely used technique for through-via filling. Electrolytic plating uses current for metal cations to transfer and form a metal layer on the conducting copper seed surface. A typical setup for Cu electrolytic plating is shown in Figure

4.9. The plating tank includes $CuSO_4$, H_2SO_4 and organic additives, such as brightener and leveler. As the direct current is applied, the cathode (glass panel) becomes rich in negative charge, and positively charged Cu cations tend to migrate towards the cathode, and are reduced to Cu to fill the TPVs. The reaction at the cathode can be written as:

$$Cu^{2+} + 2e^- \longrightarrow Cu$$

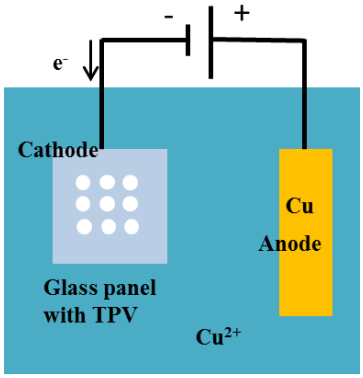


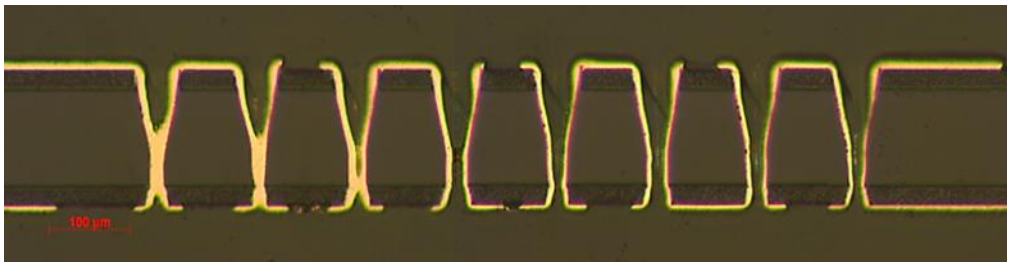
Figure 4.9. Schematic drawing of Cu electrolytic plating system

The thickness of Cu plated is governed by the equation:

$$h = 0.22 \times \text{current density (ASD)} \times t$$

where h is the plated thickness in microns, I is the current density, A is the plating surface area and t is the plating time in hours. The current density is usually presented with the unit ASD or Amperes per Square Decimeter. The current density was determined by taking into account the total surface area of the frame and the surface area of exposed copper on the sample. A Current densities of 1~3 ASD are used to ensure high quality plating inside via holes. During the plating process, the sample surface was checked at 30-minute intervals using a stylus profilometer to verify the plated Cu thickness. After plating, samples are annealed at 190^{o}C for 30 minutes to reduce stress in copper by grain growth and increase adhesion of copper to polymer.

The cross-section of the conformal plated TPVs with 60 µm diameter in 100 µm thick glass is shown in Figure 4.10. Cross-section study on the TPV arrays confirmed uniform deposition of copper on the glass surface as well as on the side-walls of TPVs. Good copper-to-via wall and copper-to-polymer adhesion was confirmed, without any interfacial failures by tape-test.



(a) **(b)**

Figure 4.10. Cross-section of TPVs after metallization with 10 µm copper plating

A metallization thickness between 3µm-10µm is necessary to enable low resistance paths for signal and power delivery through the interposer for 3D interposer applications. However, for high-power applications, thermal TPVs and for direct assembly of dies on TPV pads, TPVs need to be fully-filled with electroplated copper. Therefore, complete copper filling of TPV without voids is an important task. With direct current electroplating, it is challenging to achieve pure copper filling of vias. In order to accomplish this task, the current density and additives in the electroplating chemistry are varied accordingly, and cross-section analysis was performed to assess the size of the remaining voids. Figure 4.11 shows the decrease in void size by reducing the current density from 2.5 ASD to 1.5 ASD and by increasing the leveler content in the plating solution.

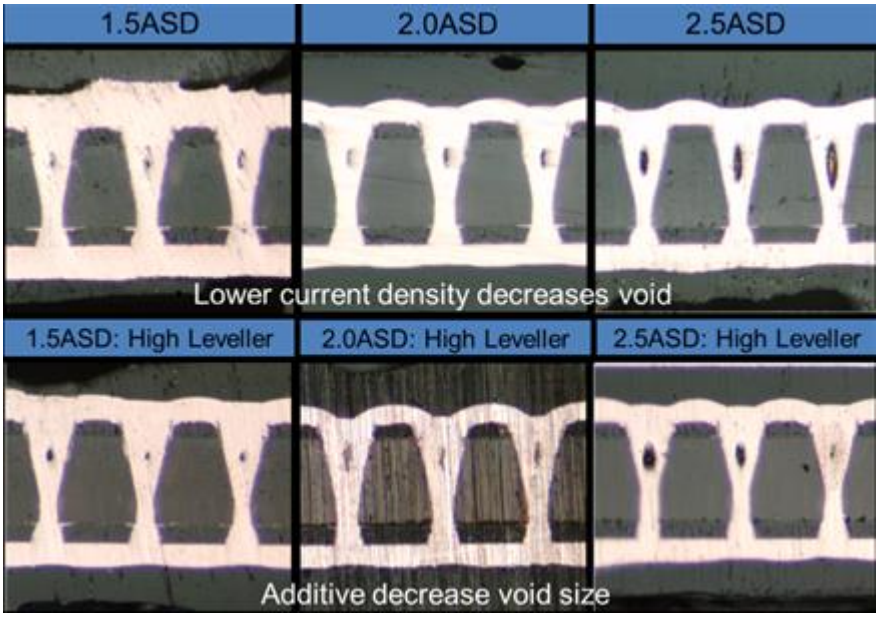


Figure 4.11. Improvement in void-free TPV plating with reduced current density and increased additives.

Therefore, using a current density of 1ASD and enabling improved solution exchange with agitation, TPVs are approximately fully-filled with copper as shown in Figure 4.12; however, small voids in the center of TPVs were still observed. Another drawback of direct current electroplating is high amount of plating on the surface. Bath chemistry needs to be further adjusted with organic additives to promote more plating inside TPV hole and slow down the plating on polymer surfaces.

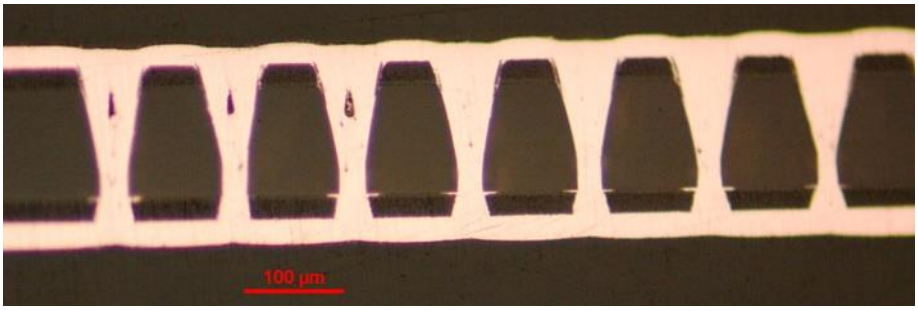


Figure 4.12. Cross-section of TPV array after copper plating with 1 ASD current density and high amount of leveler additive.

For reliability studies, TPV with such small void in the middle can be safely assumed as completely copper-filled because higher stresses occur around via ends and a small void in the middle has negligible impact on high stress around TPV corners. In order to achieve perfect copper filling of such high aspect ratio TPV structures, a two-cycle plating process can be utilized. The first cycle, with a periodic pulse reverse plating, forms a bridge in the middle of the TPV hole, followed by direct current electroplating to fill the resultant double-vias formed during the bridge cycle.

For mobile and high performance applications, subsequent build-up layers are needed to embed passive components, power-ground planes and additional signal layers to the package. Such a four-metal layer process starts with the two-metal layer stack-up, and build-up layers were fabricated using ZIF as the polymer material. The schematic process flow used to achieve four metal layer structures is illustrated in Figure 4.13.

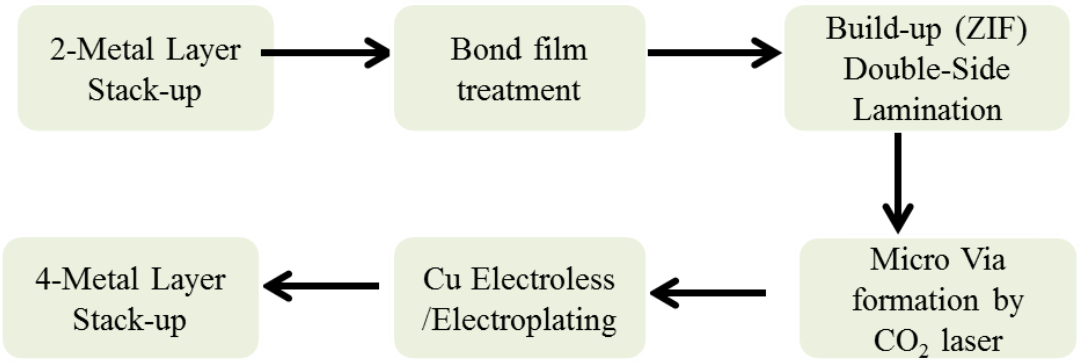


Figure 4.13.Schematic of Process flow for 4-metal layer fabrication (is it CO2 laser? Please check);

The copper on the core layers were treated with bond-film solution to roughen the copper surface and provide good adhesion between the metallization and the build-up polymer material (ZIF). A double side lamination process was then used to form the ZIF build-up layer. Due to the

flow ability of ZIF, conformal plated TPVs were filled with polymer. Next, microvias for connecting the subsequent metal layers are formed using CO_2 layer ablation. Metallization of top and bottom most metal traces and microvias are metallized again using a similar SAP process consisting of electroless plating, photoresist lamination, UV lithography and electroplating steps. The cross-section of TPVs filled inside with second build-up polymer is shown in Figure 4.14.

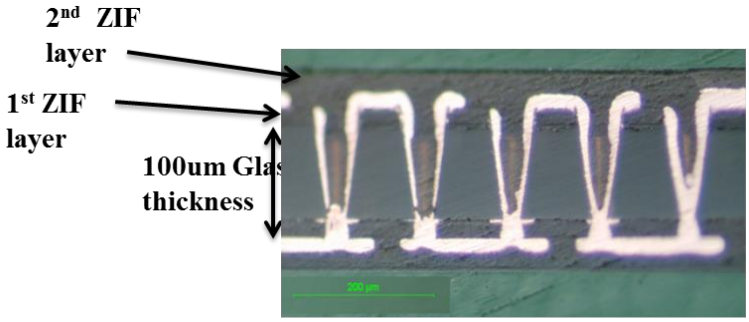
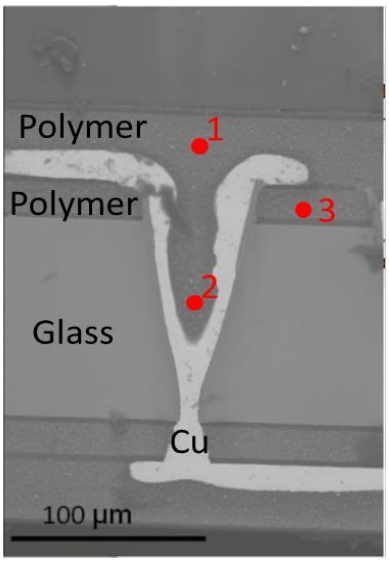
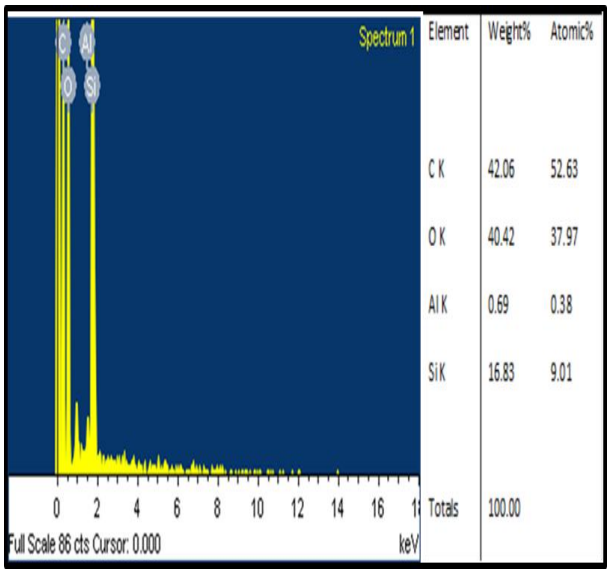


Figure 4.14. Cross-section image of polymer-filled TPV array.

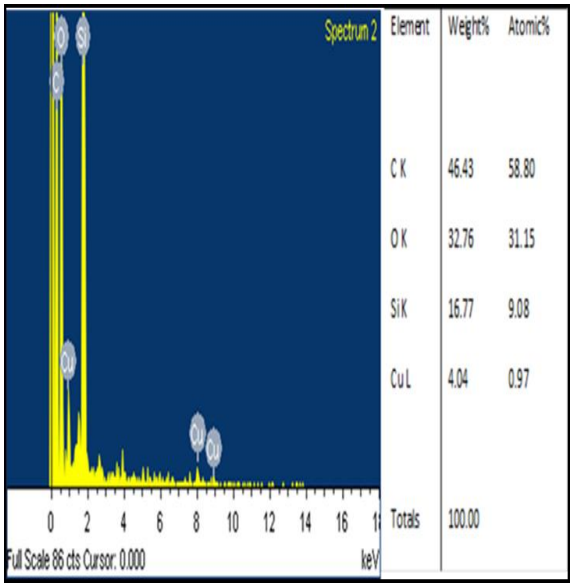
In order to confirm polymer filling inside via hole, TPV cross-section was characterized using SEM and EDS (Energy Dispersive X-ray Spectroscopy) as shown Figure 4.15.The EDS results from top surface and inside TPV hole were similar that shows successful polymer filling of high aspect ratio TPV structures.



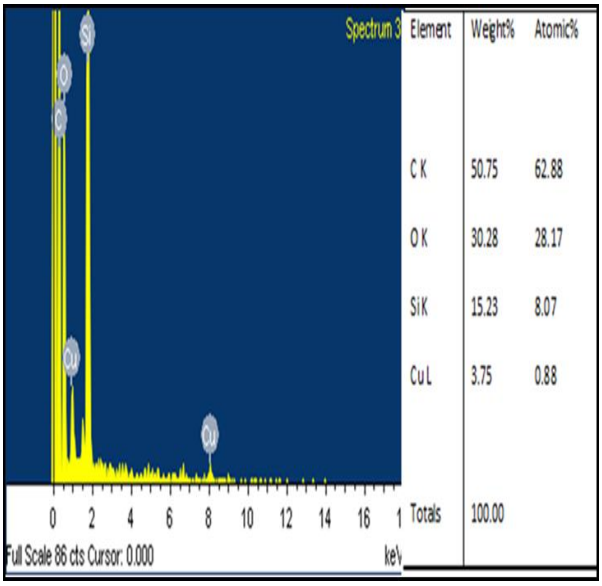
(a)



(b)



(c)



(d)

Figure 4.15. (a) SEM image of polymer-filled TPV, (b) EDS analysis from point 1, (c) point 2 and (d) point 3 demonstrating polymer filling inside depth of TPV.

The side-wall of TPVs formed by excimer laser ablation showed a thin layer of re-deposited glass. In order to understand the content inside this region, EDS analysis was used. Figure 4.16 shows the SEM images and corresponding EDS spectrums for the bulk glass and redeposited glass region inside the TPV structure. Similarity in EDS results from the two different regions confirms that the thin redeposited glass region is mainly composed of glass without polymer. During laser ablation, ablated material is vacuumed from exit region of via. Improper vacuuming leads to redeposited glass around TPV entrance.

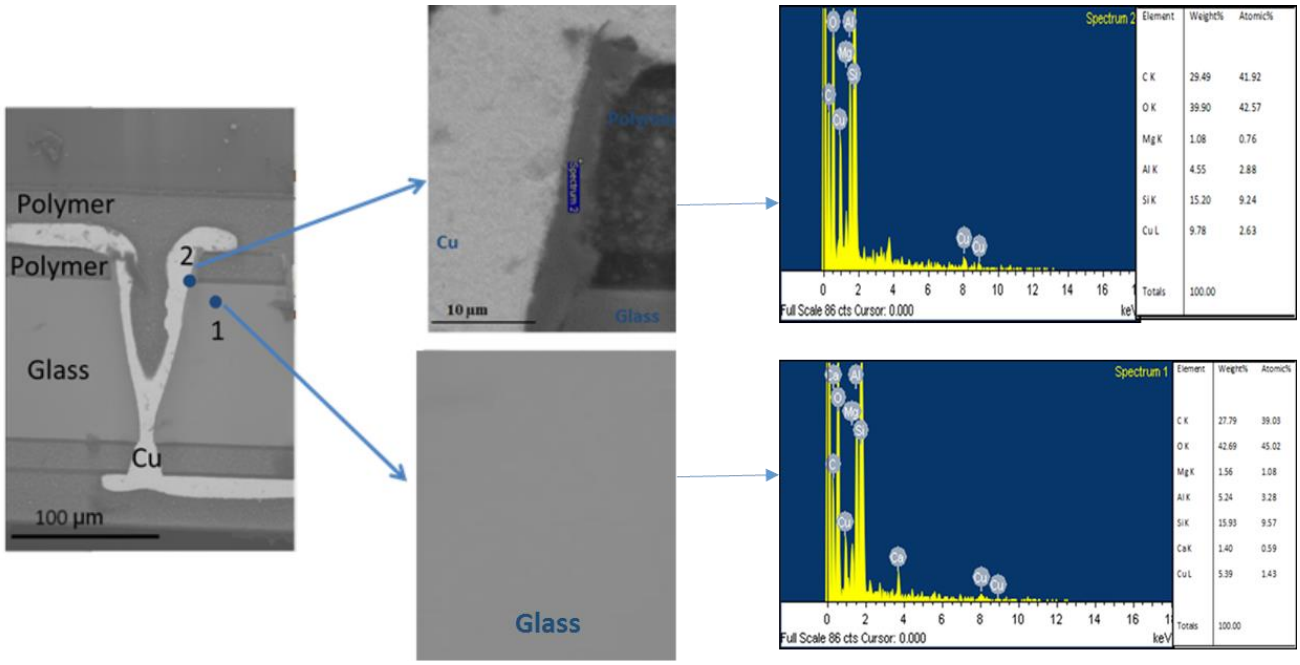


Figure 4.16. SEM cross-section of TPV with magnified images of redeposited glass and bulk glass along with corresponding EDS results

4.2. Fabrication Processes for Bare Glass Interposers

Polymer lamination on glass is a solution to address challenges with glass handling and metallization of smooth glass surfaces. Polymer fills ultra-small defects on glass surfaces, thus

increasing its strength during via-formation and subsequent processes. Low-modulus polymer also acts as a buffer layer that reduces the stress from high CTE copper on glass. Polymer films also enable metallization by acting as an adhesion-promoting layer between electroless copper and glass. In addition, polymer acts as a barrier to prevent copper migration on glass surface between high density wiring under electrical bias. However, using bare glass interposers without polymer lamination has several benefits: 1) Glass manufacturers recently developed cost-effective via formation technologies that are compatible with bare glass 2) Many polymer dielectric films decrease electrical performance due to their higher dielectric loss compared to glass 3) Direct metallization of bare glass reduces the number of fabrication steps and total thickness of interposers. Therefore, there is a compelling need to develop processes for bare glass interposer fabrication and characterization of TPV reliability.

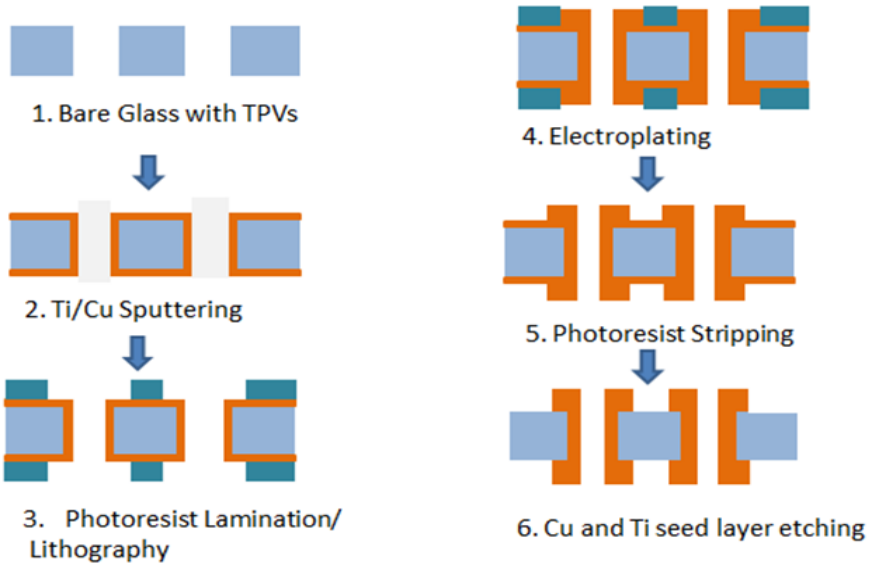


Figure.4.17. Schematic fabrication process flow of bare glass interposer

The fabrication process is presented in Figure 4.17. Bare glass panels with TPVs were provided by Corning Inc. Fig. 4.18 shows the SEM images of 30 µm diameter TPV surface and

side wall. It is seen that TPV side wall is smooth and free of microscopic defects that might act as stress concentrators initiating cracks in glass.

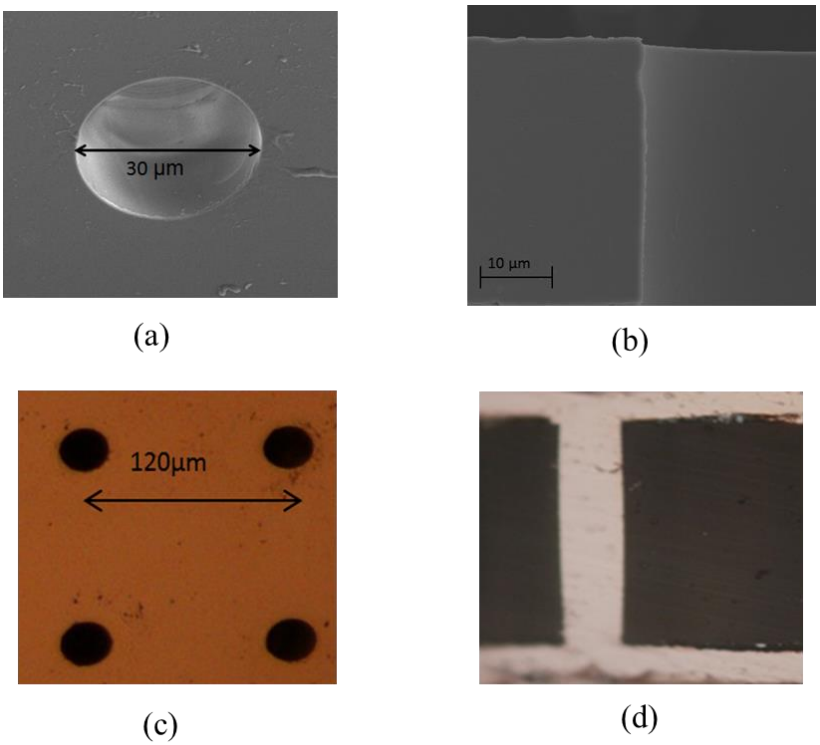


Figure 4.18. (a) SEM images of via hole with top view and (b) via sidewall, optical images of (c) top-view TPV array at 120 µm pitch and (d) cross-section of TPV after metallization

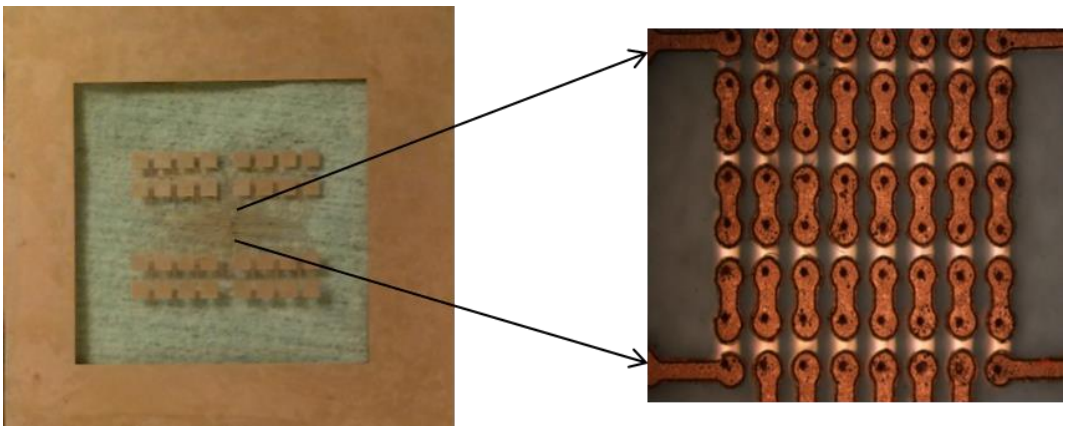
The fabrication process starts with the cleaning of the 2" panels with acetone, methanol, isopropanol, and deionized water. A Ti/Cu seed layer is then deposited by using Direct-Current Sputterer (CVC Inc.) from their high-purity targets with diameters of 3" and 8" respectively. The purpose of this seed layer is to provide the electrical contact for the electroplating process. Sputtering of high aspect ratio TPV walls with small diameter presents a challenge due to the nonconformal nature of sputtering. This challenge was addressed by applying longer sputtering times at higher power. Ti layer serves as the adhesion promoter between glass and copper. The

adhesion layer was sputtered for 20 minutes at a power of 350 W, yielding an approximate surface thickness of 100-120 nm. To prevent oxidation of deposited films and targets, the sputtering process for both layers was carried out in 100% Argon environment at a pressure of 6 mTorr.

Following the formation of Ti film, copper was sputtered onto glass at 1000 W to achieve a surface thickness of 1 μm. The reported thickness values for the Ti and Cu layers were determined for the top surface of the substrates via surface profiler (Tencor P15). Hence, the thickness of the sputtered films inside TPVs is expected to be significantly lower than the measured values. The glass panels were flipped and same sputtering process was repeated on the other side. Fairly good adhesion strength of Ti/Cu to glass was confirmed by tape test.

Following the metallization step, glass surfaces were simultaneously double-side patterned with dry film photoresist lithography process. This process consists of several steps, starting with dry-film photoresist lamination using a hot roll laminator, followed by an UV exposure, and photoresist development by dilute sodium carbonate solution in a spray tool. Upon completion of the lithography steps, electroplating of Cu was carried out in a to-electrode cell configuration. Prior to electroplating process, the panels were briefly dipped in diluted HCl solution (DI: HCL, 4:1) to remove the oxide layer on the Cu surface. An aqueous commercial Cu electroplating bath (Clean Earth Cu-Mirror Solution, Grobet) was utilized where a high purity Cu sheet of the same size and geometry as the substrate was used as the anode. The current density was set to 10 mA/ cm^2 and the solution was stirred at a moderate speed while the sample was slightly moved back and forth to ensure fresh electrolyte access to vias leading to uniform deposition within. To further improve the conformal deposition, the sample was flipped after 30 minutes of plating and plated for another 30 minutes while the back side is facing the Cu anode.

At the end of the plating process, the Cu thickness was measured to be between 8 and 12 µm on both sides of the substrate. Electroplating is followed by removing photoresist and remaining Cu and Ti seed layers. Figure 4.19 shows the top surface image of the fabricated test vehicles.



(a) **(b)**

Figure 4.19. Fabricated (a) 2”x2” test sample with TPV chains and copper wiring used for reliability characterization

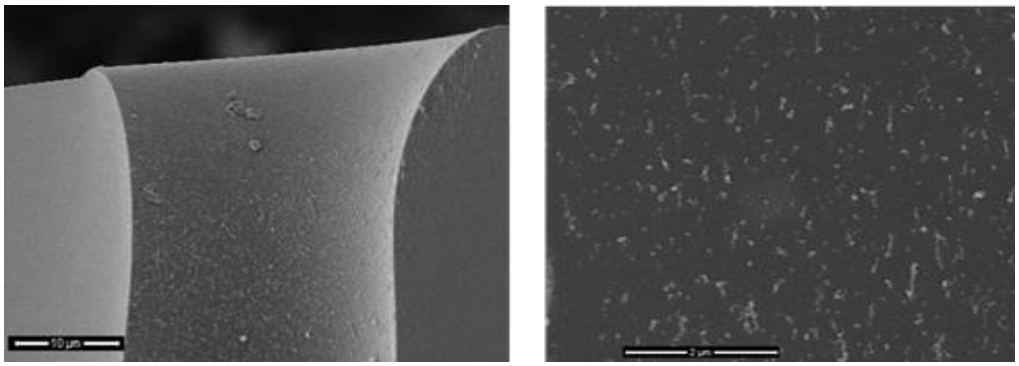
4.3. Fabrication Processes for Via-First Glass Interposers with Ultra-Thin Polymer

Laminating a polymer film onto glass, followed by TPV formation and metallization, was shown to yield a reliable structure. However, polymer lamination on glass limits subsequent fabrication steps to low-temperature processing. Lamination of glass with a polymer film prior to via formation also constraints the via-formation options to relatively harsh processes, such as laser ablation. These processes can result in damage to glass core and limit the maximum density of TPVs. In order to address the challenges with laser-via processes, innovative via-formation technologies in bare glass are being developed by substrate manufacturers. These new via-formation methods are capable of achieving smaller via diameters at smaller via pitch and are

critical to address the increasing demand for high I/O density at lower cost. These techniques are incompatible with polymer-laminated glass. However, without polymer, handling of ultra-thin glass at panel sizes become challenging. Therefore, there is a compelling need to develop and qualify glass interposer fabrication processes where vias are pre-fabricated before any glass panel processing. Such TPVs have glass/Cu interfaces on via side-walls while the top surface has glass/polymer/copper.

In this section, an innovative low-cost via-first process that is scalable to ultra-small and high aspect ratio TPVs with low glass and interfacial stresses is developed to address the challenges with laser via formation after polymer lamination and direct glass metallization. It utilizes a thin polymer film that is laminated onto the glass with vias, and subsequently patterned. This polymer acts as an intermediate layer between glass and copper to mitigate handling and reliability challenges due to CTE mismatch between copper and glass. This approach also replaces the sputtering step with electroless plating.

Fabrication process starts with bare glass panel with vias that were formed by electrical discharge process on 6" bare glass panels of 100 μm thickness from Asahi Glass Co. Via formation occurs by focusing a controlled electrical discharge current to create locally molten region of glass, followed by dielectric breakdown and removal of glass. With this process, via diameters of 20 μm at 50 μm pitch can be achieved. For test vehicles in this study, through-vias with 60 μm entrance diameter at 220 μm pitch were used. SEM image of TPV cross-section before fabrication process is shown in Figure 4.20.



(a) **(b)**

Figure 4.20. SEM images of (a) TPV entrance, (b) TPV wall

Curvature at via entrance was observed. TPV wall was free of defects and cracks that can act as stress concentrators. In via sidewalls, roughness in range of few nanometers was observed that can provide adhesion by mechanical anchoring of electroless copper onto bare glass. The fabrication process is shown in Figure 4.21.

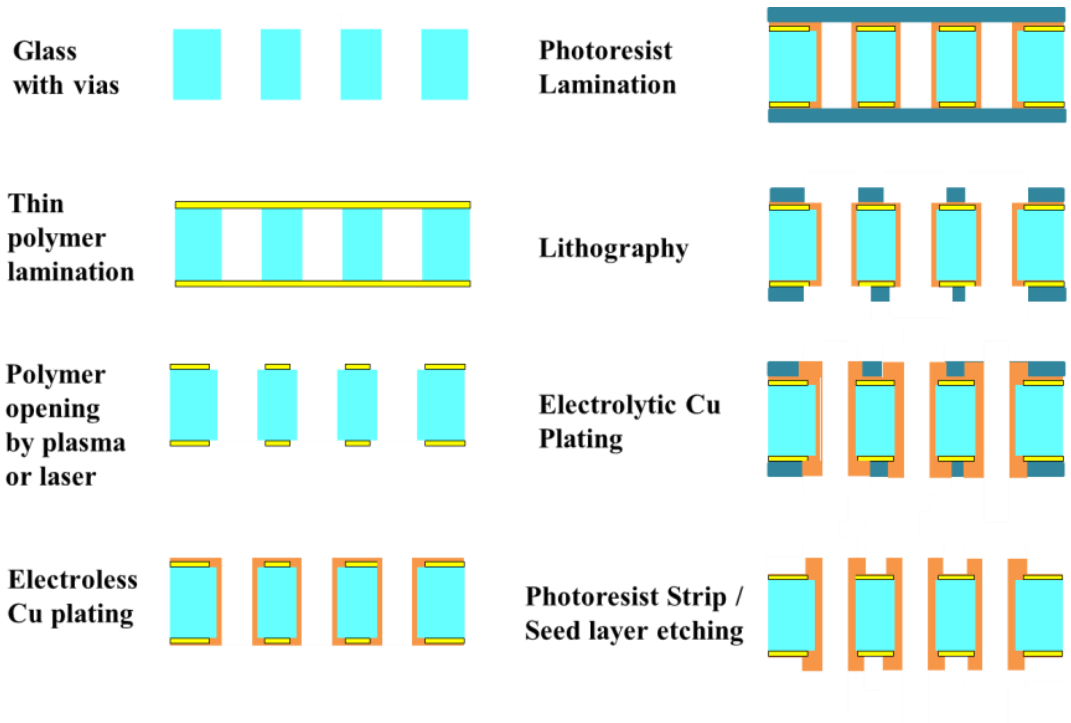


Figure 4.21. Via-first fabrication process-flow for test vehicles

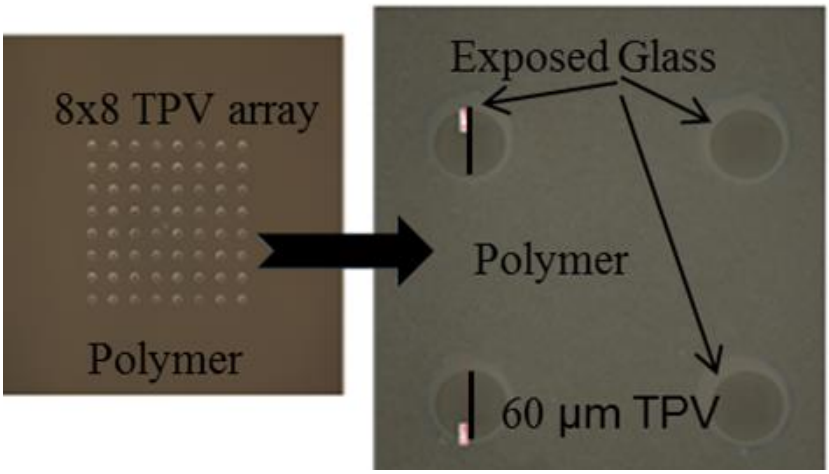
The fabrication process starts with cleaning of bare glass panels with vias using acetone, methanol, isopropanol, and deionized water. The panels were also subjected to O_2 plasma cleaning step to remove any surface contamination. Next, glass surfaces were treated with a silane solution (3-aminopropyltrimethoxy silane) to create covalent bonds at the interfaces between polymer and glass to increase adhesion strength. Ajinomoto Buildup Film GX92 with 5 µm thickness was used as the dryfilm polymer dielectric [89]. The material properties of the GX-92 film is given in Table 4.4.

Table 4.4.Material properties of ABF GX92 Polymer

Properties	**Unit**	**ABF GX92**
T_g (DMA)	^oC	168
CTE	ppm/ ^oC	39
Water Absorption (100^oC 1hr)	wt%	1
Elongation	%	5.6
Dielectric Constant (Dk)	(1~10 GHz)	3.2
Loss Tangent (Df)	(1~10 GHz)	0.017
Lamination Temperature	^oC	120
Young's Modulus	GPa	5
Laser Process-able	-	Yes

Prior to lamination step, in order avoid the flow of uncured polymer into vias, polymer films were pre-cured at room temperature for 12h, followed by heating at 100 ^{o}C for 20 min. Polymer films were simultaneously laminated onto both sides of glass using a vacuum laminator. This double-side process eliminates possible issues with warpage of thin glass panel during polymer lamination process and during heating and cooling cycles. This step also minimizes damage during glass-handling. Polymer lamination step ends with by thermal curing of the film at 190^{o}C for 90 minutes.

After polymer lamination, the via hole needs to be opened by removing the thin polymer layer. This is achieved by either plasma etching or laser. During plasma etching, polymer area outside of via holes needs to be protected by an etch mask. Polymer opening by laser doesn't require that protection, thus simplifying the process; however, laser has the potential to create damage on glass. In this study, polymer areas over TPV holes were opened with plasma etching. Dry film photoresist was laminated onto the substrates and with a photolithography step, photoresist over via areas were photopatterned to expose the polymer underneath. The exposed polymer was etched by RF plasma (400W power) of O_2 and CF_4 gas at 100^{o}C for 15 min. If the process is not well-controlled, the excess removal of polymer results in a ring of exposed bare glass around TPVs, as illustrated in Figure 4.22.



(a) **(b)**

Figure 4.22. Top view optical image of (a) 8x8 TPV array, and (b) TPVs after polymer opening with damage.

After patterning of polymer films, seed layer formation for metallization of TPVs and wiring layer is achieved by electroless plating. Both sides of panel were then laminated with dry-film photoresists and patterned with UV lithography. Subsequently, electrolytic plating using a semi-additive process method was performed in order to deposit approximately 10 µm copper on both surfaces. Fabrication was completed by photoresist stripping and micro etching the electroless seed layer. Cross-section of the fabricated test structures is shown in Figure 4.23. Taper is observed in TPV structures, with an approximate entrance diameter of 60 µm and an exit diameter of 45 µm, also curvature on both sites. There is no material debris on entry and exit sites.

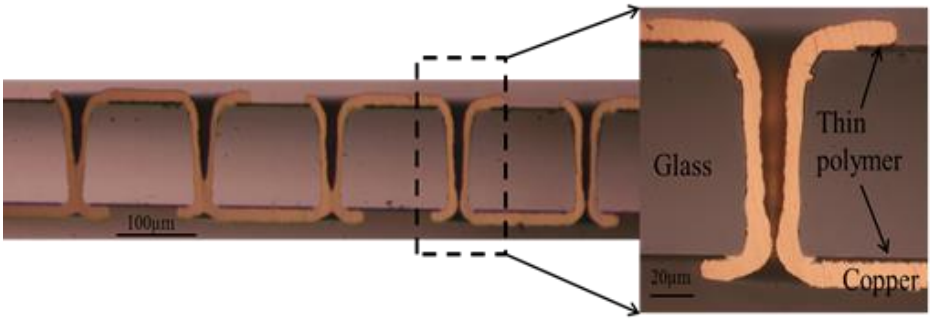


Figure. 4.23. Optical image of TPV test structures after fabrication

4.4. Fabrication Processes for Glass Interposer with Double-Side Assembly

The real benefits of ultra-thin glass interposers are, seen with double-side or 3D assembly of active and passive components on glass. Assembled components on both sides introduce different thermomechanical loadings resulting in global and local strains on TPVs. Furthermore, the process defects during glass via formation and copper plating create additional reliability concerns. Therefore, there is compelling need to fabricate test structures to characterize reliability of TPV in 3D package with double-side IC assembly. The fabrication process is shown in Figure 4.24. This process is based on the substrate passivation using a dry solder mask resist and electro-less nickel immersion gold (ENIG) metals surface finish.

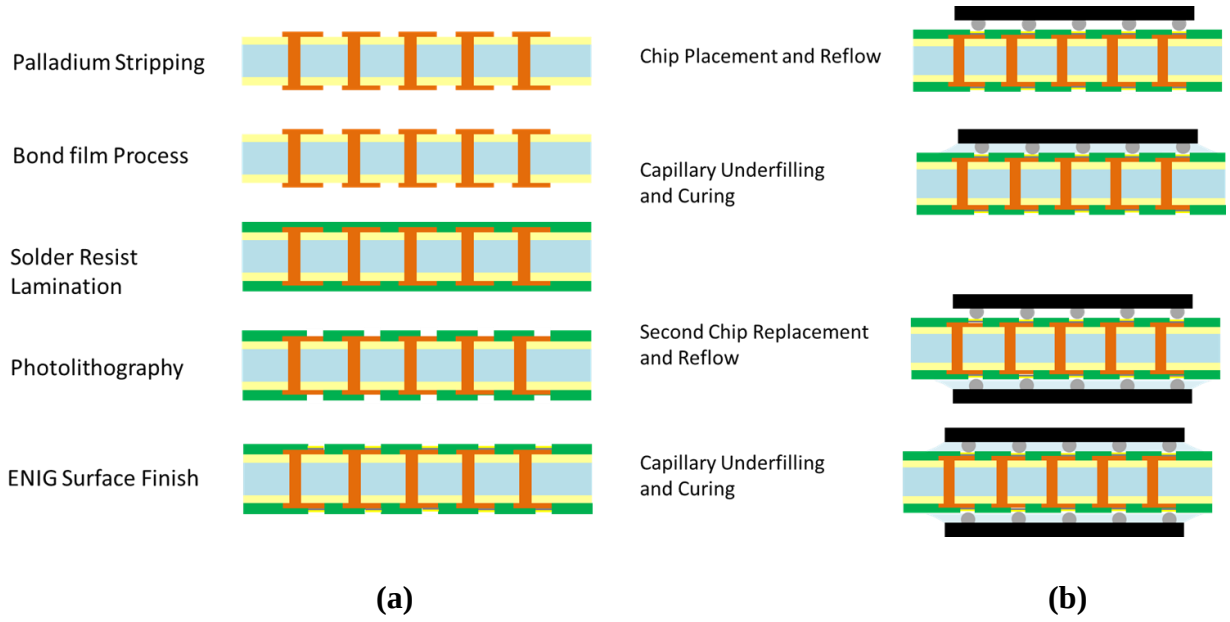


Figure 4.24. Schematic process flow (a) surface passivation and (b) double-side IC assembly.

Fabrication process starts with metallized polymer-laminated glass interposers. This requires passivation of surfaces, followed by surface preparation for IC assembly with a metal surface finish. Both these steps are performed to protect the RDLs and the contact pads. Before implementing these two steps, any palladium residue from electroless plating step was removed by dipping the panels into palladium stripper at 50^{o}C. Prior to solder resist lamination, bond film process was applied onto the glass interposer to roughen the copper surface to promote adhesion of solder resist to copper via pads and RDL. Solder resist was laminated simultaneously on both sides using vacuum laminator. Solder resist was patterned using UV lithography, developed, and thermally cured at 150^{o}C for 60 minutes. Electroless nickel and gold (ENIG) surface finish was applied so that the gold layer prevents oxidation of substrate pads while nickel acts as a barrier

between solder and copper to control intermetallic growth and enhance reliability. After this step, interposers were mechanically diced to individual coupons for IC assembly.

Flip-chip test dies were sequentially assembled on both sides of glass coupons by solder reflow, followed by applying underfill and curing to avoid movement of first assembled IC during second reflow. Test dies had its own flipchip solder ball array with a diameter of 115 µm using a lead-free Sn-Ag-Cu alloy. Capillary underfill also mitigates stresses induced in solder balls due to CTE mismatch between glass and die. BGA land pads before assembly, and x-ray and optical image of test coupons after die assembly are shown in Figure 4.25.

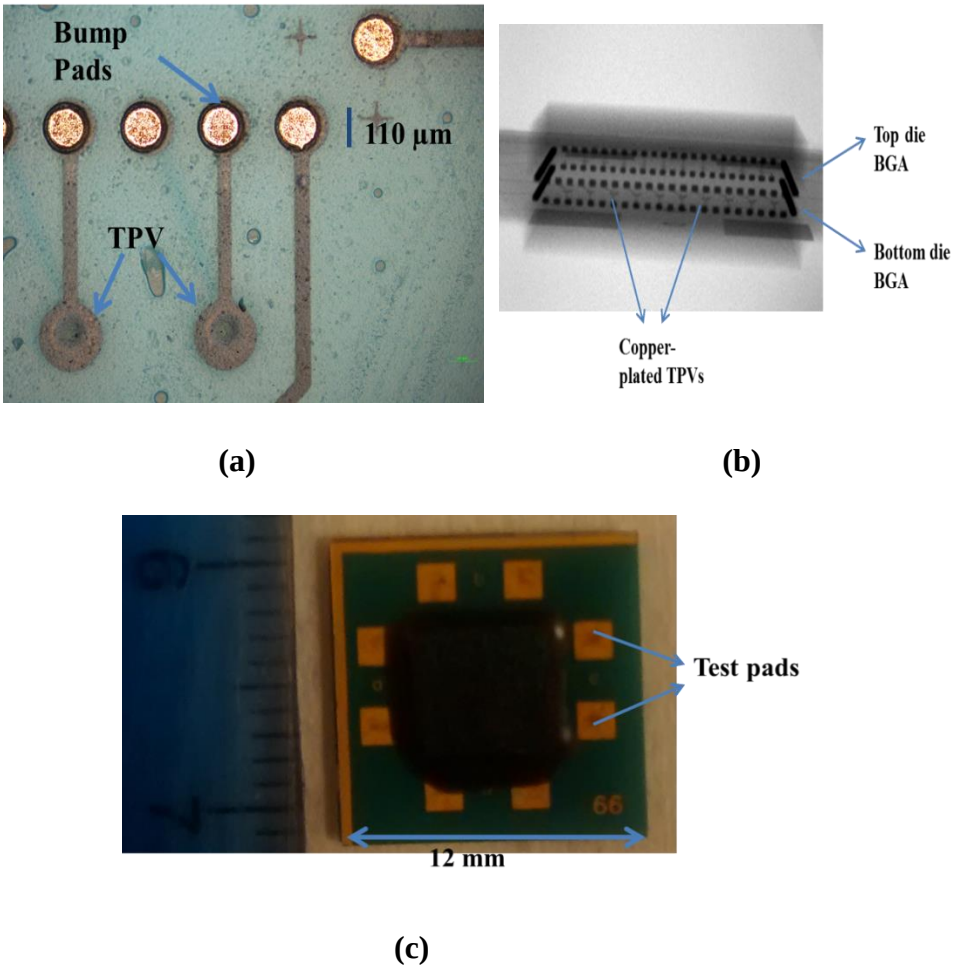
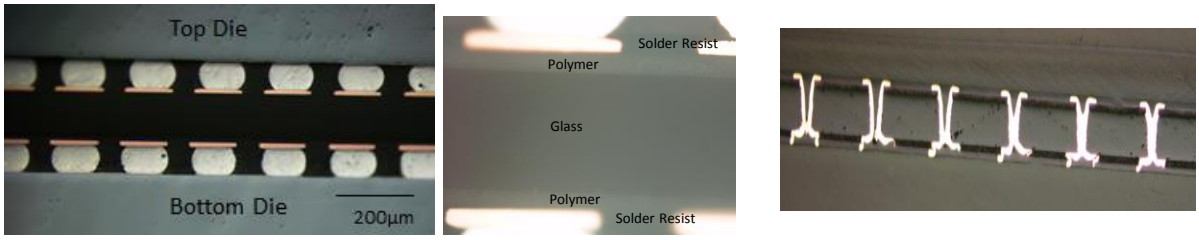


Figure 4.25. (a) BGA land pads and Glass interposer with coupons after assembly (b) X-ray image of test coupon

Cross-sections of test vehicles depicting solder bumps and TPV array after glass interposer fabrication and assembly are shown in Figure 4.26. The TPV hole formation was performed using a 355nm UV laser.



(a) **(b)** **(c)**

Figure 4.26. (a) Cross-section of a representative test vehicle with double-side assembly (b) Cross-section of the interposer showing the pad and solder resist, and (c) TPV Array after double-side assembly.

CHAPTER 5

RELIABILITY CHARACTERIZATION OF TPVs

This chapter describes the design and reliability characterization of test vehicles in order to validate the thermomechanical models and the predicted failure modes from Chapter 3, and validate the design rules. Following the design guidelines from Chapter 3, TPVs are designed and fabricated for high reliability in free-standing glass and with assembled dies using the fabrication processes described in Chapter 4. Based on the design guidelines, geometry and materials of TPV test-vehicles are determined. These test vehicles consist of various TPV transitions with daisy chain structures. Test vehicles are designed to characterize TPV reliability in both DC and RF domain. In addition, four-point probe pads (Kelvin structures) are included in the design. Resistance monitoring was carried during the thermal cycling tests. Scanning Electron Microscopy imaging was conducted to analyze the samples and identify the failure modes.

Section 1 describes the design of test vehicles used for reliability characterization. Section 2 summarizes the conducted reliability tests. Section 3 presents the reliability characterization of TPVs in polymer-laminated glass formed with via-last process using ArF excimer, UV and CO_2 lasers with varying via diameter and glass thicknesses. Section 4 describes the reliability of TPVs formed with laser-assisted chemical etching in bare glass. In Section 5, test-results from TPVs in thin polymer-laminated glasses that are formed with the via-first process are discussed. Section 6 focuses on reliability of TPVs in 3D package. Section 7 describes direct stress measurements on glass and TPVs using Micro Raman spectroscopy. Section 8 summarizes the findings in this chapter.

5.1 Design of Test Vehicles

Resistance of single TPVs and array of TPVs can be obtained from DC measurements. However, the measurement method needs to be sensitive to small changes in resistance due to thermomechanical stresses. For such measurements, test vehicles are designed with 4-point probe (Kelvin probe) pads. DC 4-point probe measurements enable to accurately determine the resistance of a single TPV and TPV arrays by eliminating the resistance errors from the connecting wires and the contact resistance between probe and pad.

The four-point probe method, or Kelvin method, as depicted schematically in Figure 5.1, involved the use of both an ampermeter and a voltmeter. Because of the voltmeter's high resistance, the inner loop ideally does not draw any current, leading to a voltage reading that is nearly the same as if it were connected directly across the subject resistance. Hence this method is able to exclude any errors from probe contact resistances and wire resistances. And the resistance of the device under test (DUT) can be simply written as $R_{chain} = \frac{Voltmeter\ Indication}{Ampermeter\ Indication}$ where R_{chain} is the resistance of TPV daisy chain.

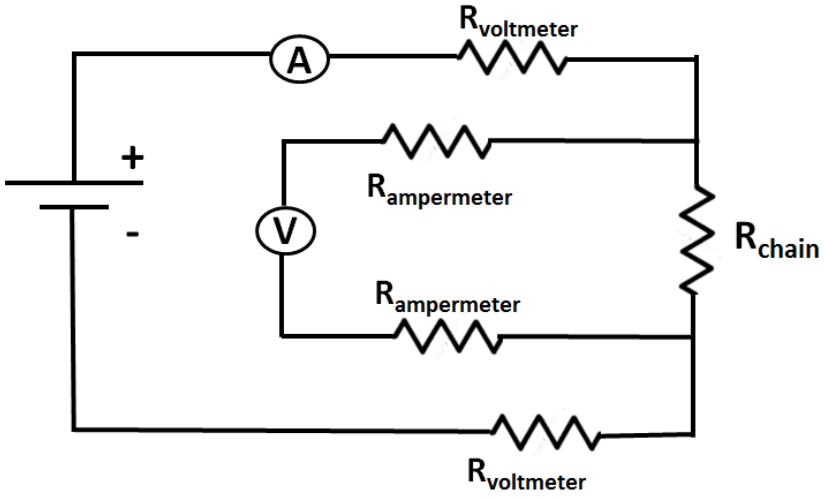
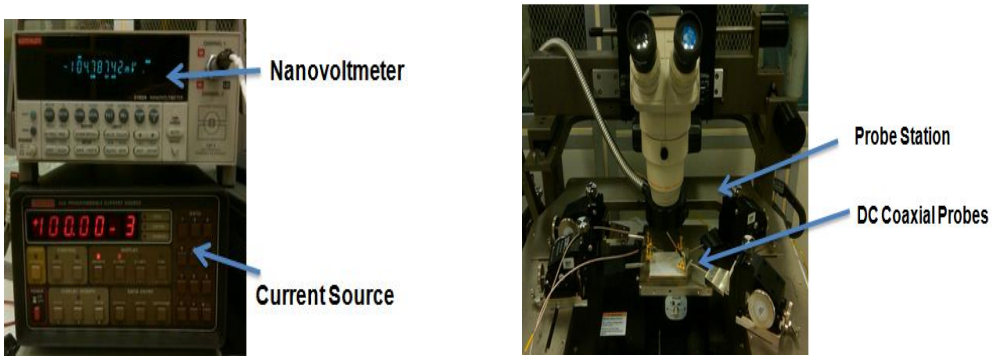


Figure 5.1. Schematic circuit drawing for four-point probe method

The 4-point probe system is shown in Figure 5.2. The system is calibrated with two reference resistors with resistance values of 5 mΩ and 0.5mΩ to control sensitivity and the calibration results are shown in table 5.1.



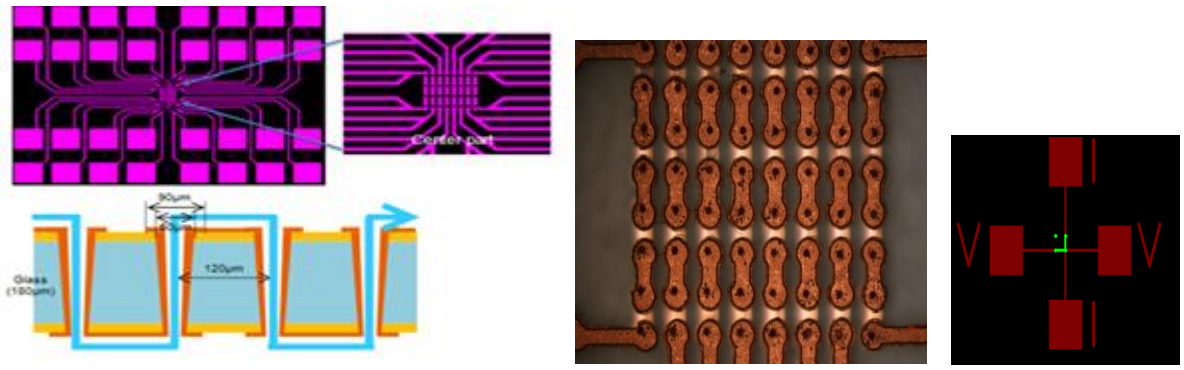
(a) **(b)**

Figure 5.2. (a) Nano voltmeter and precision current source (b) Probe station

Table 5.1 Calibration of 4-point probe measurement system.

	Measured Resistance	**Accuracy**
5.0mΩ	5.0081mΩ	0.16%
0.5mΩ	0.5052mΩ	1.01%

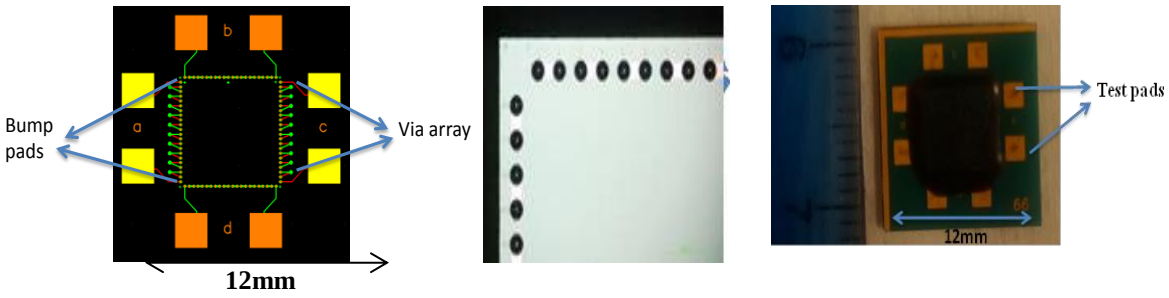
DC-based test vehicles are designed to accurately measure resistance of TPV daisy chains and single TPVs. TPV daisy chains and Kelvin structure for single TPV are shown in Figure 5.3.



(a) **(b)** **(c)**

Figure 5.3. (a) TPV chains with Kelvin probes (b) TPV chain (c) Kelvin structure for single TPV

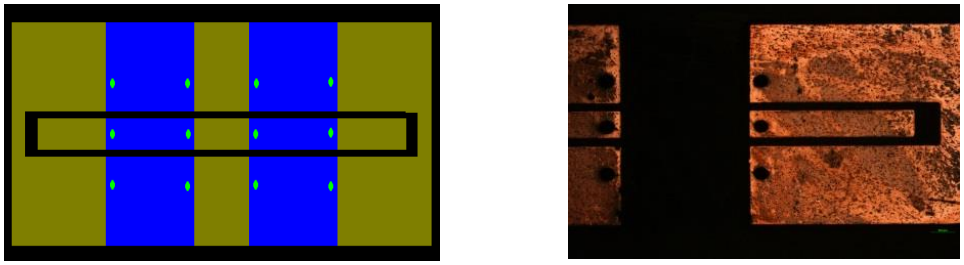
Another DC-based test vehicle design for assessing the reliability of TPVs in 3D assembly is shown in Figure 5.4. This design is based on daisy-chains formed from top die solder bump, TPV and bottom die solder bump. The resistance of the chain consisting of 22 solders bumps and 10 TPVs is measured through probe pads. When any interconnection in this daisy chain fails, the whole daisy-chain fails. This design enables to test reliability of both solder bumps and TPVs simultaneously.



(a) **(b)** **(c)**

Figure 5.4. (a) 3D Assembly test vehicle design (b) flip-chip test die (c) Assembly test vehicle

RF-based test vehicles are designed in order to assess the reliability of TPVs in RF path and to utilize the sensitivity of s-parameters against possible defect growth in TPV. For determining and optimizing the CPW performance, HFFS models are built and simulated. Based on the models, CPW (coplanar waveguide) structures with varying number of via transitions are designed and fabricated as shown in Figure 5.5.



(a) **(b)**

Figure 5.5. (a) CPW with TPV transitions design and (b) portion of fabricated test vehicle

5.2 Reliability Tests

Increasing the temperature range is one of the methods to accelerate failure occurrences when performing thermal cycling for reliability evaluation. This is because failure mechanisms are induced in a much shorter duration. In order to qualify thermomechanical reliability of TPVs, test vehicles were thermal cycled between hot and cold extremes. The test vehicles were first subjected to a 24-hour bake at 125°C, followed by accelerated moisture sensitivity level 3 (MSL-3) preconditioning (60°C, 60% RH for 40 hours), and three times reflow at a peak temperature of 260°C, to simulate the lead-free board assembly processes. This preconditioning identifies the possibility of polymer delamination or cracking of copper due to popcorn effect from rapid evaporation of absorbed water molecules. The test vehicles were subjected to thermal cycles

between -55°C and 125°C with a dwell-time of 15 minutes at each temperature extreme, as described in JEDEC JESD22-A104 condition B test standard using a Thermotron 7800 oven. The samples were taken out at specific intervals. Daisy chain resistances for DC-based test vehicles, and scattering parameters (s-parameters) of transmission lines for RF-based test vehicles, were measured to detect TPV failures. Significant changes in electrical resistance for DC-based test vehicles and in s-parameters for RF-based test vehicles are chosen as the failure criteria.

For some test vehicles, in addition to thermomechanical reliability, the electrochemical migration reliability of TPVs was also investigated using biased highly-accelerated temperature and humidity stress test (biased-HAST). This test has been previously used to investigate the electrochemical reliability of through-vias in glass fiber reinforced organic package substrates with different bias voltages**.** The test setup consists of a HAST chamber, to produce 130^{o}C and 85% humidity required for the test. A source/measurement unit (Keithley 236) was used to apply the voltage and measure the output current. The test vehicles were first subjected to a 24 hour bake at 125^{o}C, MSL-3 preconditioning (60^{o}C, 60% RH and 40 hours), followed by 3-times reflow at 260 ^{o}C, and then subjected to biased-HAST (130^{o}C, 85% RH and 5V DC bias) for 100 hours as per JEDEC JESD22-A110 test standard. Insulation resistance was recorded periodically and a drop in resistance to 50 kΩ was used as the failure criteria. Following the design rules from Chapter 3 and fabrication processes from Chapter 4, test vehicles are fabricated to assess the thermomechanical reliability of TPVs formed with different formation methods in various configurations. Fabricated test vehicles are summarized in table 5.2.

Table 5.2 Summary of Fabricated Test Vehicles

Glass Thickness(μm)	TPV Diameter(μm)	Metallization Type	TPV Formation
TPV in Free-Standing Polymer-Laminated Glass			
180	60	Conformal	Excimer Laser
100	60	Conformal	Excimer Laser
100	60	Fully-filled	Excimer Laser
30	30	Conformal	UV Laser
100	60	Conformal	UV Laser
100	60	Conformal	CO2 Laser
TPV in Free-Standing Bare Glass Test Vehicle			
100	30	Ti/Cu Sputtering and conformal plating	Laser-Assisted Chemical Etching
300	100	Conformal	Laser-Assisted Chemical Etching
Via-First TPVs in Glass with Thin Polymer			
100	60	Conformal	Electrical Discharge
TPV in 3D Assembly Test Vehicle			
100	60	Conformal	UV Laser
100	60	Conformal	UV Laser

This task describes the analysis of TPV defects after via formation, metallization and thermal cycling. The purpose of this analysis is to assess the growth and impact of initial defects on reliability of TPVs formed with different methods. Cross-sections of TPV holes fabricated

with different methods are prepared by dicing glass substrates. Cross-sections of metallized TPVs are prepared by epoxy molding, grinding and polishing.

5.3 TPVs in Free-Standing Polymer-Laminated Glass

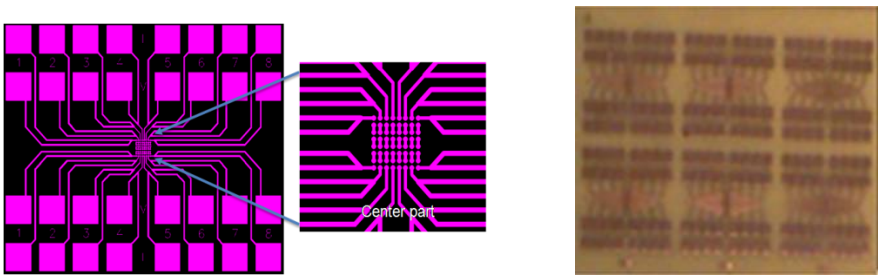
5.3.1 ArF Excimer Laser

In this TPV formation method, 193nm ArF excimer is used to break the bonds in glass. Following the fabrication processes described in Chapter 4, various test vehicles were fabricated as listed in table 5.3.

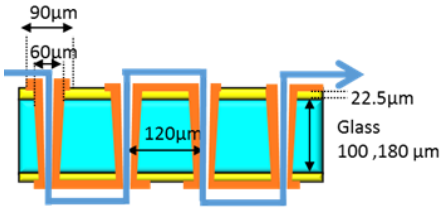
Table 5.3 Fabricated TPV structures

Via Diameter (µm)	Glass Thickness (µm)	Metallization Type
60	180	Conformal
60	100	Conformal
60	100	Fully-filled

Test vehicle for investigating thermomechanical reliability of TPVs utilizes daisy chain structures of through-package-vias as shown in Figure 5.6 along with the fabricated test structures. Each test coupon has 64 TPVs arranged in an 8x8 matrix. Each TPV chain is connected with a four-point Kelvin-Probe structure to enable sensitive resistance measurements without the influence of contact and trace resistances. The test vehicle is designed for a TPV diameter of 60µm and pitch of 120µm.



(a) **(b)**



(c)

Figure 5.6. (a) Test vehicle layout, (b) example of fabricated coupons, and (c) schematic of connected TPV arrays.

The SEM cross-section of TPVs in glass before metallization is shown in Figure 5.7 Taper in TPV was observed with narrowing via diameter from laser beam entry to exit. There was slight accumulation of ablated glass debris around the entry region. As laser ablation process does not melt glass, TPV sidewalls had some visible roughness and grooves. These small defects along the via sidewall can provide mechanical anchoring of copper, resulting in better adhesion and thus increased reliability. These defects can also create stress concentrations; however, defect sizes are very small in nanometer range that may not lead to sufficiently high stress intensity factors for fracture of glass. A simple risk assessment can be made as follows: Assuming fracture toughness of glass as 0.5 MPa $m^{1/2}$, stress around TPV corners approximately 125 MPa as predicted from modeling, and mode I type fracture under uniform tension with an edge defect, critical defect size can be roughly estimated using $K_I = \sigma\sqrt{\pi a} \times 1.12$ where K_I, σ and a are fracture toughness, critical stress and defect length respectively. Critical defect size is approximately 4 µm from this equation, which is substantially higher than laser-ablation

defects. Moreover, stresses attenuate quickly with increasing distance from the TPV end. Stresses also attenuate quickly with distances far away from the glass/copper interface. However; it is still critical to experimentally demonstrate reliability of TPVs fabricated using this novel panel-based process.

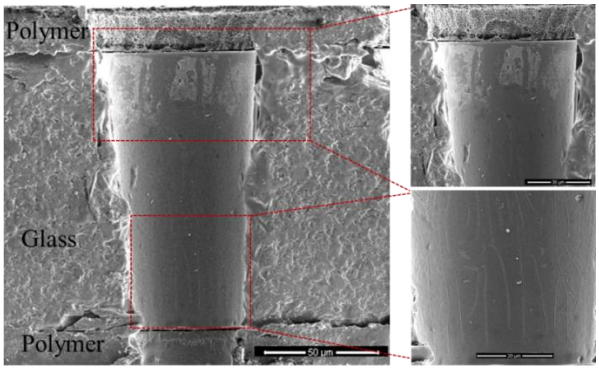
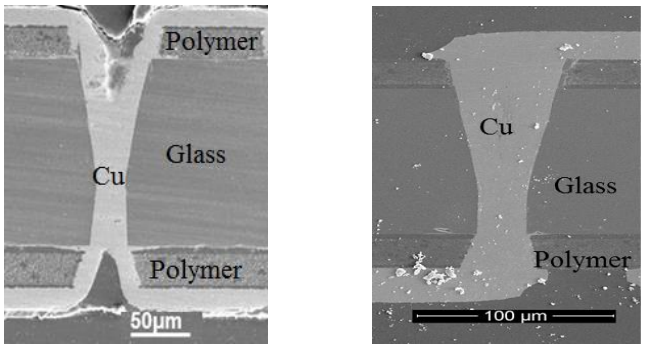


Figure 5.7. SEM image of TPV cross-section, showing glass debris on TPV entry side, and roughness and grooves on via wall

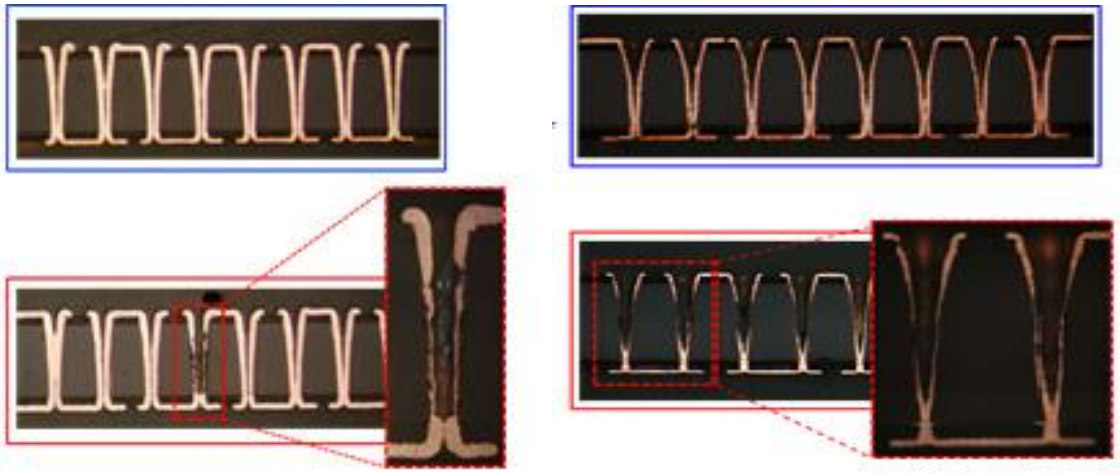
TPVs are plated both partially-filled and fully-filled. Furthermore, polymer filling of partially-filled TPVs was performed to assess its impact on TPV reliability. Cross-sections of partially- and fully-filled TPVs are shown in Figure 5.8.



(a) (b)

Figure 5.8 Cross-sections of TPVs after metallization with 10 µm copper plating and (b) fully-filled

The fabricated structures were first subjected to MSL-3 (moisture sensitivity level-3) preconditioning, which included a 24-hour bake at 125^{o}C followed by storage in a humidity chamber of 60% RH at 60^{o}C for 48 hours, and followed by 3 times reflow. Test vehicles were then cycled from -55^{o}C to 125^{o}C with a dwell time of 15 minutes at each extreme. Test vehicles were subjected 4000 thermal cycles as in JEDEC (JESD22-A104 condition B) test standards to evaluate the reliability of TPV with varying dimensions. The resistances of daisy chains were measured at regular intervals. A resistance change of more than 10% of initial resistance was chosen as the failure criterion. In total, 136 daisy chain structures made up of 1088 TPVs were subjected to thermal cycling test. Minority of daisy chains in 180 µm glass failed the thermal cycling in 100 cycles, which can be considered as infant failures. Failure analysis was performed by cross-sectioning the samples to expose the TPVs. The samples were molded in order to protect the glass samples from cracking during cross-sectioning. The molded samples were polished to expose the TPVs. A passed TPV array and a failed TPV array corresponding to the same material combination (ENA1/RXP-4) are compared in Figure 5.9. Among 8 TPVs, the plating defect in one TPV led to disconnection of the TPV chain in 100 cycles. Similarly, metallization process defects in the whole TPV chain led to ultra–thin copper plating on the via wall, which could not withstand thermomechanical stresses from CTE mismatch.



(a) **(b)**

Figure 5.9. Passed TPV chain (top) vs failed TPV chain (bottom) with metallization defect in (a) single via and (b) whole chain

As the imperfection in the plating process increases, reliability of these structures decrease. So care should be taken to have uniform electroplating in the fabrication process to demonstrate reliable microvias. The infant failures in TPV chains are directly related to the plating defects, especially thinner or discontinuous copper layer on via walls. Moreover, this thin copper leading to high resistance was detected from 4-point resistance measurements. The DC resistance of a conformal plated TPV can be theoretically calculated using the following equation:

$$R = \int_0^h \left(\frac{\rho_{cu}}{2t_{cu}.\pi \left[\frac{(a-b)x}{h} + b - 0.5t_{cu} \right]} \right) . dx \qquad \text{Equation (5.1)}$$

where t_{cu} and ρ_{cu} correspond to the thickness of the conformal metal and resistivity of copper respectively; ‘a’ and ‘b’, represent the radii of exit and entrance side of TPV. The value of ‘h’ indicates the total height of the TPV, which is 220 µm for the fabricated test vehicle. Theoretical TPV resistance was calculated using this equation with the following values:

a = 60 µm, b = 60 µm, h = 220 µm, t_{cu} = 10 µm and ρ_{cu} = 1.72 x 10^{-2} Ωµm.

Using this formula, for a uniform plating of 8 TPV chains, resistance can be approximately calculated by summing eight TPV resistances with the corresponding copper line resistance by the following equation $R = \rho_{cu} \times \frac{L}{W \times t_{cu}}$ where L refers to total length of copper lines connecting TPVs to the probe point and W refers to copper line width. Approximated daisy chain resistance for this test vehicle can be calculated by substituting L = 480 μm and W = 60 μm. The resistance is calculated to be approximately 100mΩ.

The above calculation estimates the resistance of a normal TPV daisy chain with uniform copper plating. Using this approximation, it is thus possible to predict TPV chains with abnormally higher resistance due to irregularities such as non-uniform or discontinuous copper plating. These resistances can be detected with 4-point measurements. Resistance of passed TPV arrays were in the range of 100-300 mΩ whereas failed TPV arrays show a resistance value above 400 mΩ indicating poor copper coverage inside TPV. This is illustrated in Figure 5.10. Plating defects that can cause reliability concerns can be identified using 4-point resistance measurements. The resistance of via chains is also shown as an indicator of plating quality, which is directly related to their reliability. Through-via plating process can be easily improved by optimization of plating bath agitation and by decreasing the aspect ratio by reducing glass interposer thickness. With decrease of glass thickness while keeping the diameter constant, the plating process defects can be eliminated.

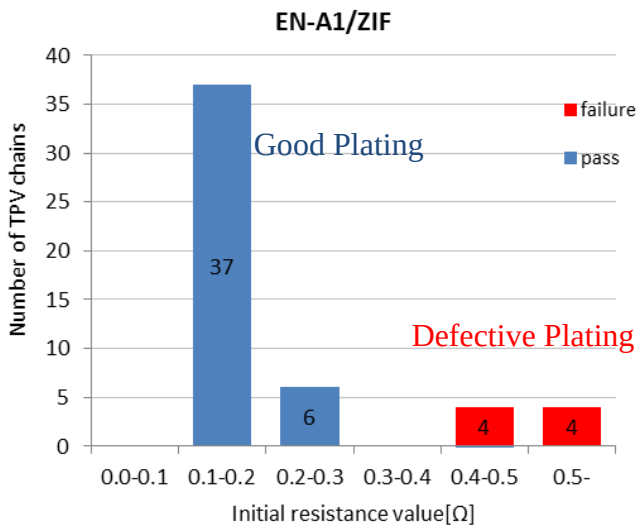


Figure 5.10. Resistance values for daisy chains with good and defective plating for EN-A1/ZIF material combination. Blue also indicates good plating, while red indicates defective plating.

All daisy chain structures consisting of 8 TPVs without any metallization defects passed 4000 thermal cycles with a stable resistance between 100-200mΩ, confirming the thermomechanical reliability of TPVs in glass. This result is expected as the fatigue life was estimated to be higher than 10000 thermal cycles from thermomechanical simulations. The cross-section of TPV array in 100 µm glass before thermal cycling is shown in Figure 5.11. Redeposited glass is observed around the entrance of TPV. During via drilling, ablated material is vacuumed away through the exit side of the TPV. Therefore, redeposited glass is more likely to exist in the entrance region. Secondly, delamination of polymer from glass was observed on exit side of the TPV.

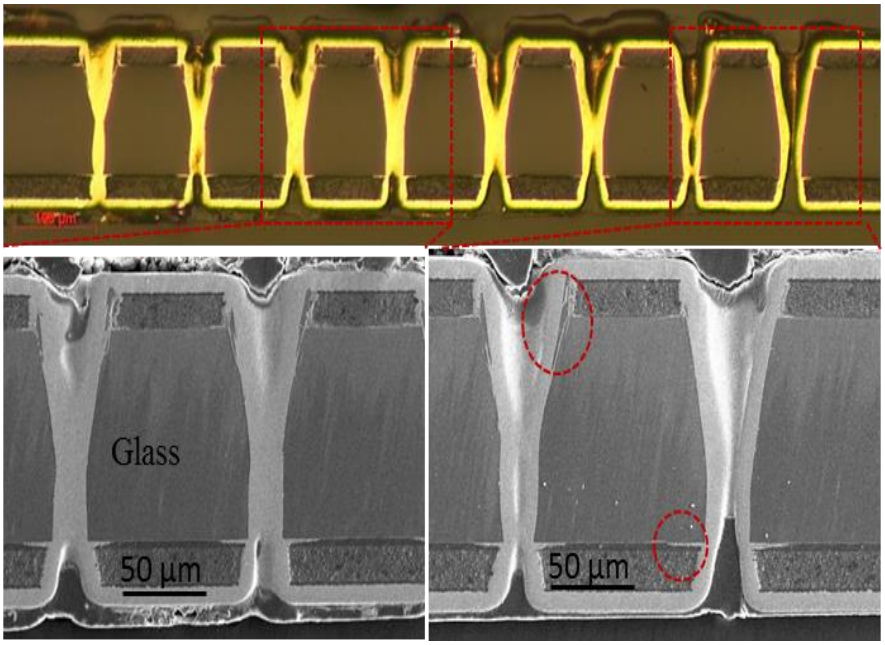


Figure 5.11. ArF excimer laser-drilled TPV array after fabrication: redeposited glass and polymer-delamination are circled

Cross-section of TPV array after 4000 thermal cycles is shown in Figure 5.12. As seen in the figure, TPV array didn't show any visible degradation after the reliability testing. Redeposited glass around TPV entrance that may create high stress concentrations, didn't lead to cracks in copper due to the high fracture toughness of ductile copper. High fatigue life of copper, as predicted from modeling, explains the absence of failures even after 4000 thermal cycles. No crack growth was observed even in the high-stress areas of glass such as via corners, presumably because of small process defects. Also, polymer delamination on exit side of TPV didn't grow due to the low energy release rate for crack growth, as expected from FEM simulations. This can also be explained by low interfacial tensile stresses (also referred to as peeling stresses) in y direction and high adhesion between polymer and glass due to silane treatment, as explained in fabrication process. Additionally, delamination of copper from TPV wall due to peeling and shear stresses was not observed. This can be related to the roughness in the TPV wall created

during laser drilling. This roughness leads to higher adhesion strength between copper and glass wall. An average roughness of 50 nm provides sufficient adhesion to copper to pass tape test.

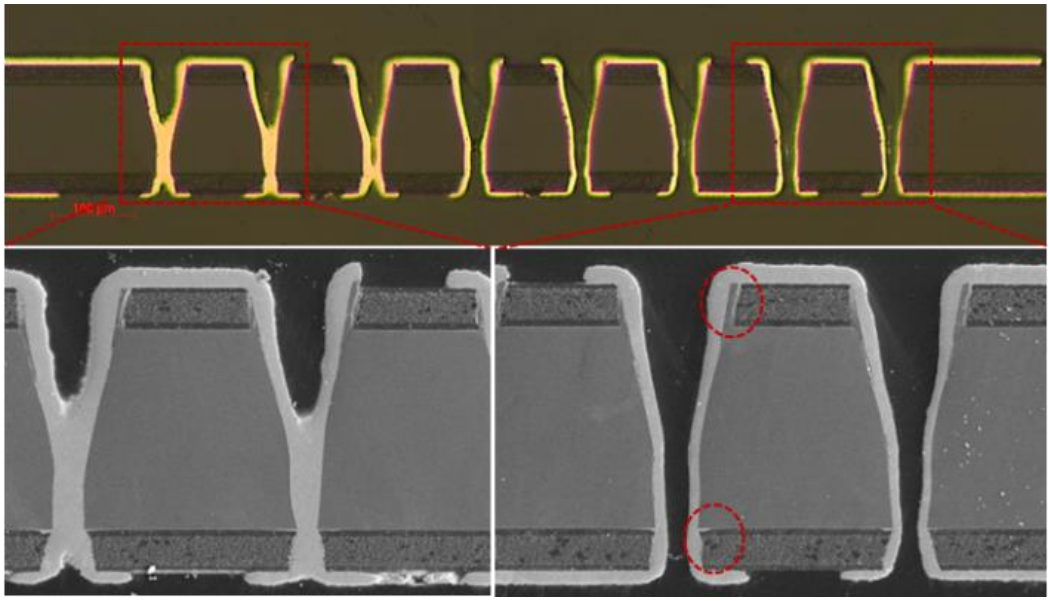


Figure 5.12. ArF excimer laser-drilled TPV array after fabrication, redeposited glass and polymer-delamination are circled

After 8000 thermal cycles, resistance increase was observed and related to crack growth in copper at the copper-glass-polymer corners around the exit region, as shown in Figure 5.13, where there is high deformation as predicted from mechanical modeling.

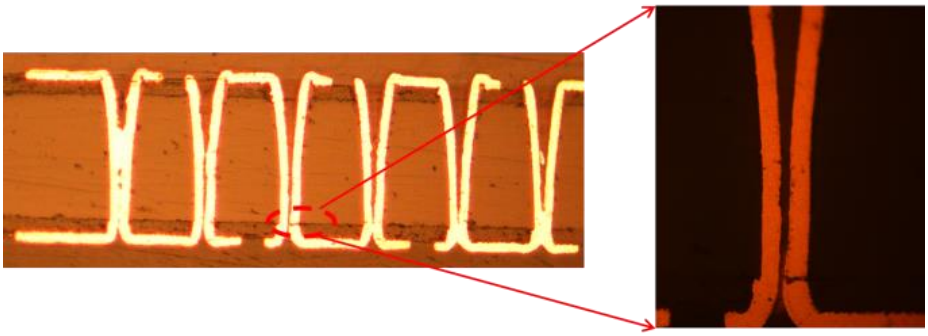
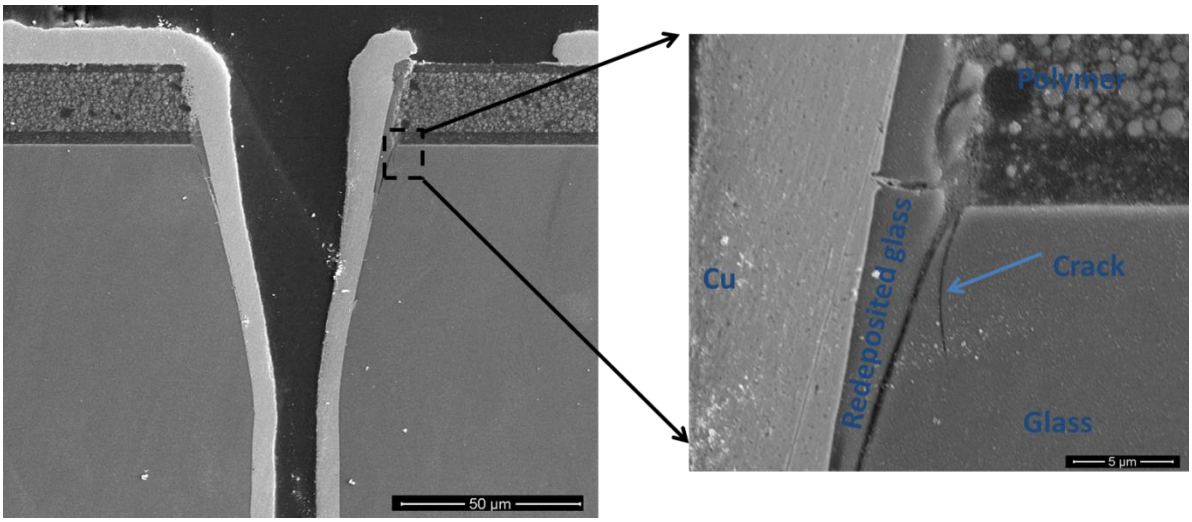


Figure 5.13. Crack growth in copper at the polymer-glass interface at the TPV exit region, leading to increase in resistance

In some TPVs, crack in glass around TPV entrance region was observed, as shown in Figure 5.14, possibly created during laser ablation. As the size of the crack is small and thermomechanical stresses are not high enough, it didn't grow during thermal cycling as predicted by FEM modeling.



(a) **(b)**

Figure 5.14. (a) Glass cracking around TPV entrance and (b) magnified view

Cross-section of fully-filled TPV after 4000 thermal cycles is shown in Figure 5.16. Due to the high copper content, thermomechanical stresses on glass are higher, which can drive growth of cohesive or interfacial cracks. However, this failure mode was not observed even in the TPV corners where high stresses are predicted from modeling. This indicates the thermomechanical reliability of TPVs fabricated with this novel process in these geometries.

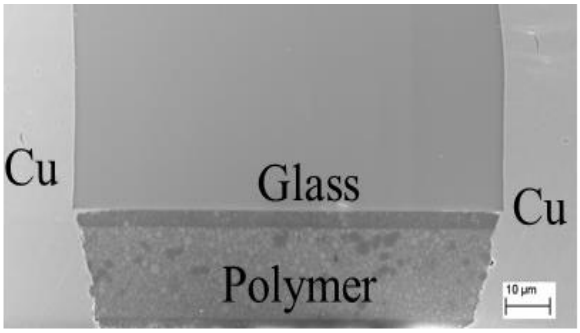
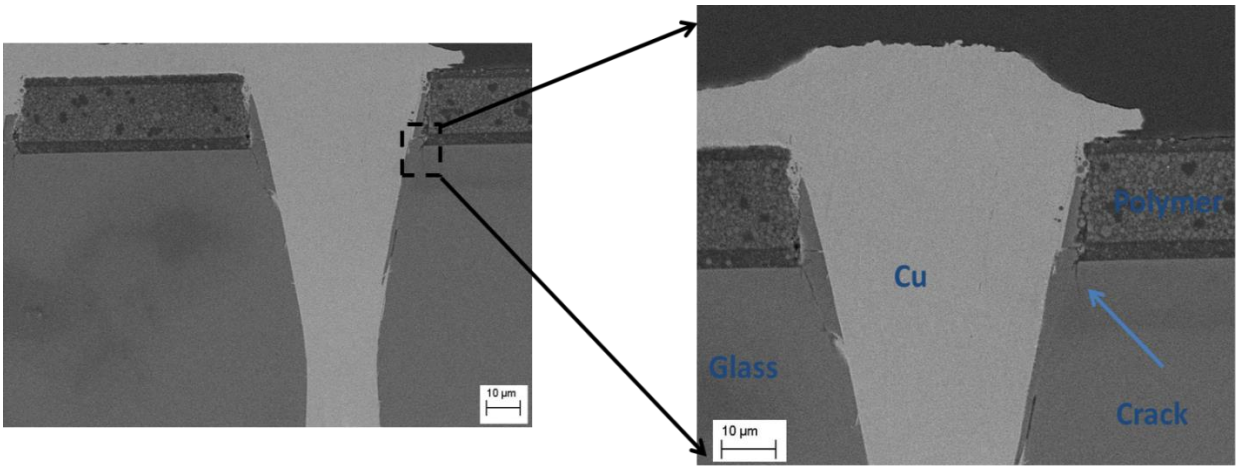


Figure 5.15. Fully-filled TPV corner around via exit region after 4000 thermal cycles, showing no crack in glass, no growth of polymer/glass delamination or copper delamination in via sidewall

As in partially-filled TPVs, some TPVs exhibit crack around entrance at the polymer-copper-glass junction as shown in Figure 5.16. However, even with higher thermomechanical stresses compared to conformal TPVs, these cracks didn't grow with thermal cycling as predicted by FEM simulations in Chapter 3.



(a) **(b)**

Figure 5.16. (a) Glass cracking around TPV entrance and (b) magnified view

In some TPVs, delamination of copper from polymer was observed vertically and horizontally as depicted in Figure 5.17 that were not observed with partially-filled TPVs. This

can be attributed to the higher thermomechanical stresses and the variation of adhesion strength between copper and polymer among the panel. Figure 5.18 shows a similar interfacial crack in polymer/copper interface and polymer/glass interface. The adhesion strength of copper to polymer can be increased by creating higher roughness with desmear process. The initial delamination of polymer from glass on TPV exit side didn't grow during thermal cycling due to the high bonding strength between polymer and glass, and low peeling forces, as predicted by modeling.

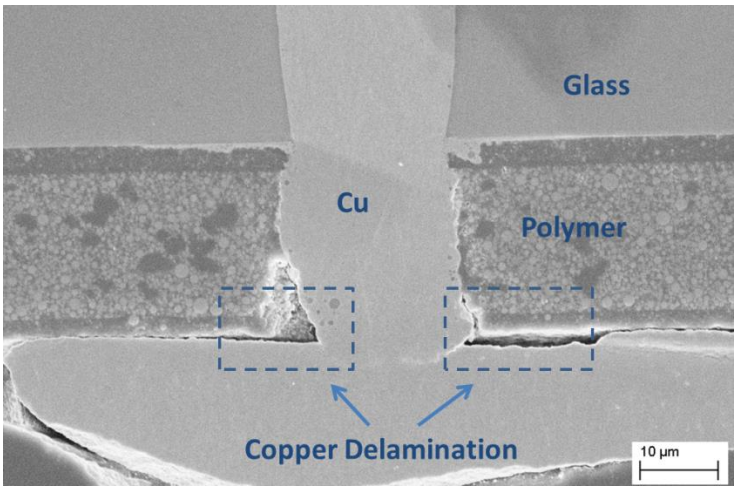


Figure 5.17. Delamination of copper from polymer both in vertical and horizontal direction

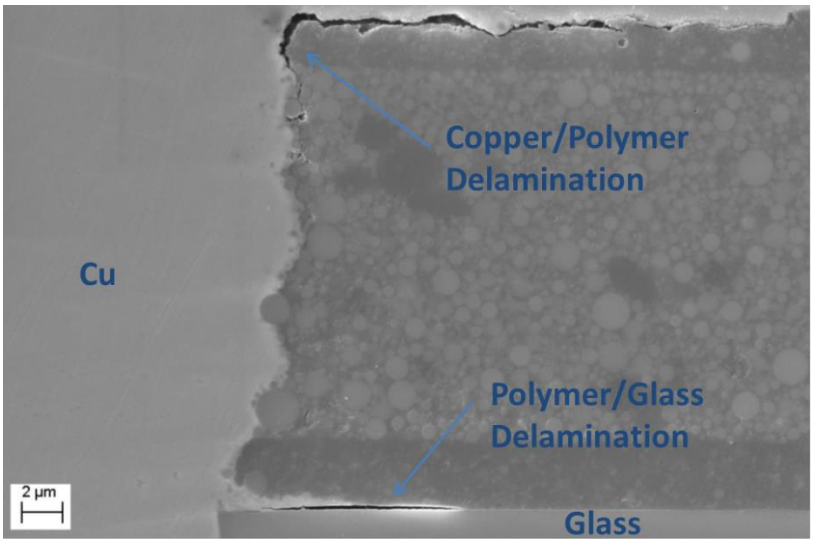


Figure 5.18. Interfacial delamination in copper/polymer and polymer/glass interfaces

5.3.2 UV Laser

The SEM cross-section of TPVs drilled with UV laser in glass before metallization is shown in Figure 5.19. As UV laser creates extensive heat accumulation during via formation, polymer damage was observed mainly in the exit region. Similar to excimer laser, taper in via was observed. Furthermore, roughness in via walls is high; however, defect sizes were not observed to be higher than 5 µm.

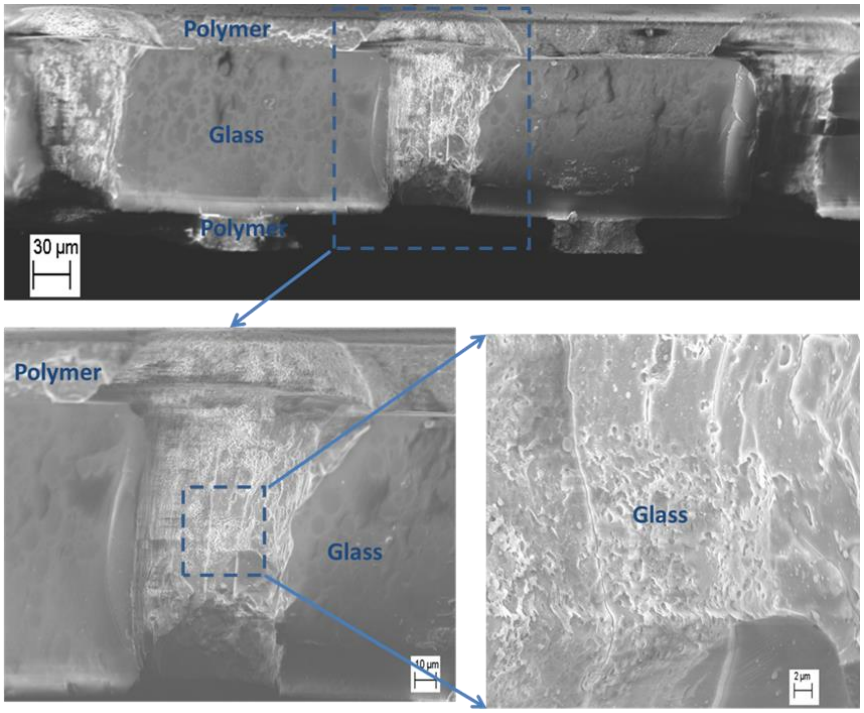
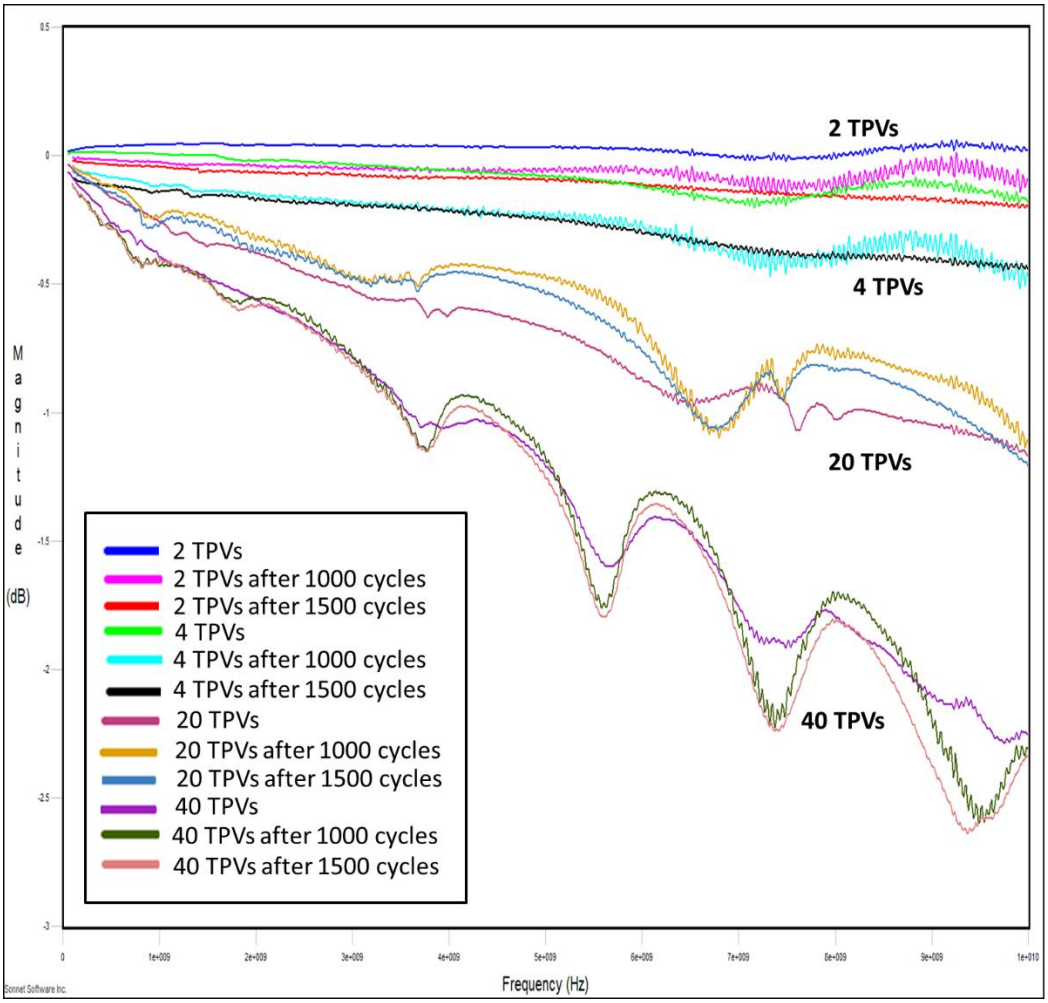


Figure 5.19. SEM image of TPV cross-section drilled with UV laser

As observed in the previous reliability tests, monitoring DC resistance does not give much information about changes in TPV structure with thermal cycling. Therefore, s parameters of CPW transmission lines were monitored in RF domain up to 10 GHz. As RF signals are more sensitive to changes in the structure, impact of thermal cycling was assumed to be more profound. To characterize the reliability of TPV in RF range, transmission lines with varying number of TPV transitions are designed and fabricated as described. As expected from simulations, higher number of TPV transitions lead to higher loss, thus lower s12 values as illustrated in Figure 5.19.

The test samples were subjected to thermal cycling test and s-parameters were measured at 1000 and 1500 cycles. The results are shown in Figure 5.20. Small changes in s12 parameter were observed with thermal cycling. These are attributed to the calibration of VNA.

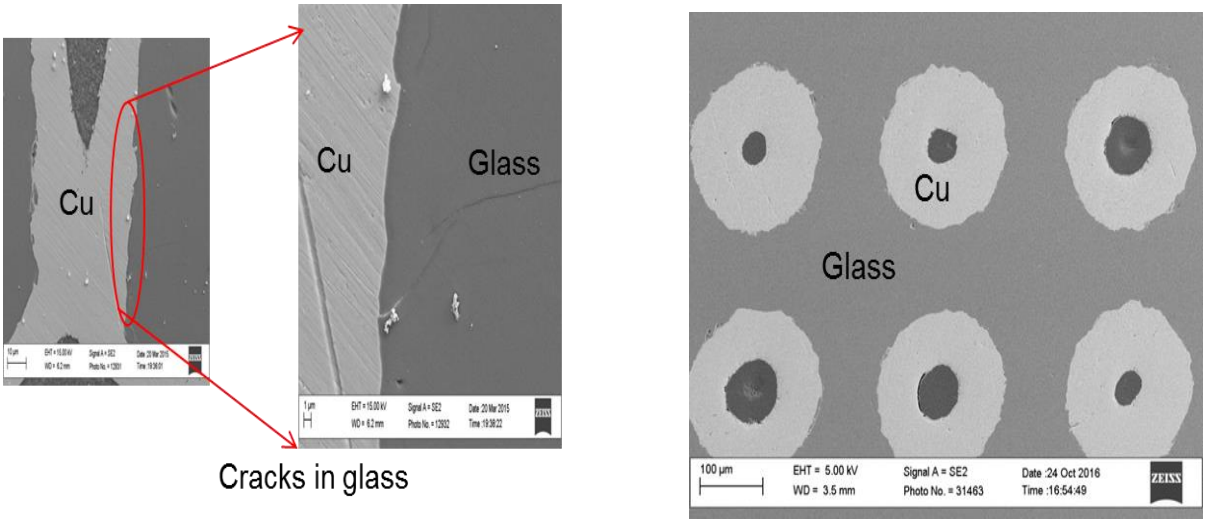


(b)

Figure 5.20. Parameter S12 values in dB of CPW lines with varying TPV transitions after thermal cycling.

Figure 5.21 and Figure 5.22 illustrate the failure analysis revealing cracks in glass which can be related to the high defect density and size along the TPV wall. As expected from simulations, despite large defects, radial cracking in glass was not observed as TPV diameter is smaller than 100 µm and plating is conformal. Cracks in TPV corner was also observed which is

related to the high stress concentration. As in TSVs, these cracks were looping back to the copper/glass interface [48].



(a) **(b)**

Figure 5.21.(a) Crack formation in TPV wall , (b) no radial cracks

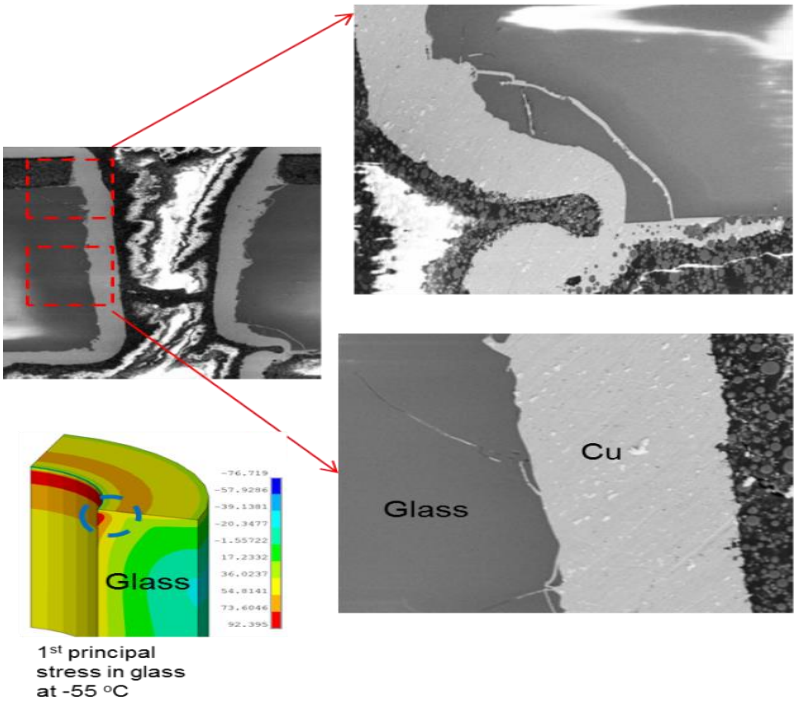


Figure 5.22. Cracking along TPV wall and glass corner where high stress is expected from modelling

5.3.3 CO_2 Laser

A number of test vehicles were fabricated to investigate the reliability of the CO_2 laser-drilled TPVs with 60 µm dimeter at 120 µm and 200 µm pitches. The test vehicles were TPV daisy chains with four contact pads in order to conduct 4-point probe resistance measurements. Test vehicles were fabricated using the polymer-laminated glass interposer fabrication process described in Chapter 4. In both the cases, 100 µm thick glass substrates with 22.5 µm thick ZIF polymer layers were used on both sides.

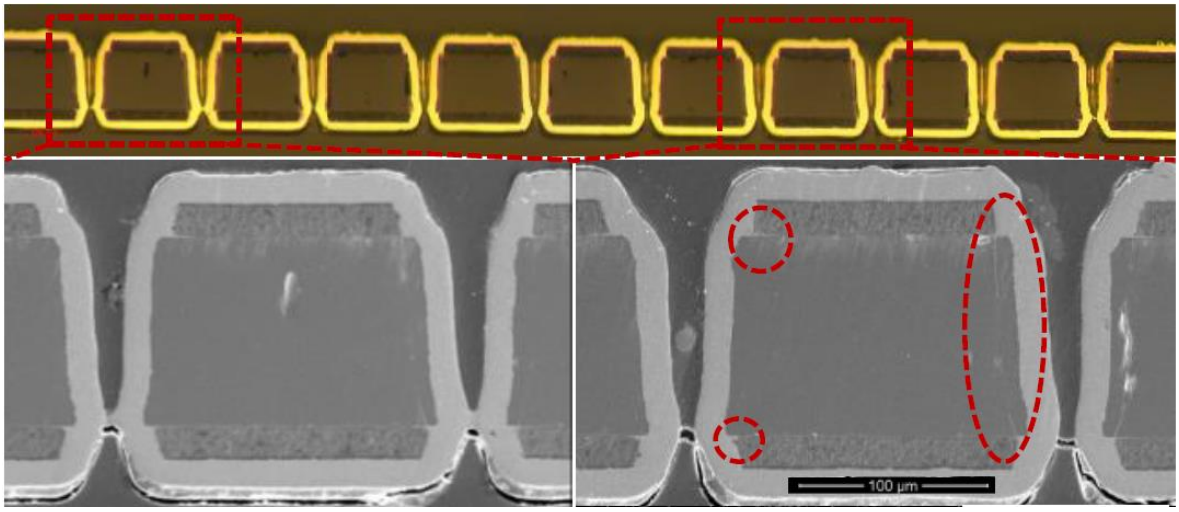


Figure 5.23. Optical and SEM micrographs of CO_2 laser-drilled TPVs test vehicle. Cracked at the interface between heat-affected zone (HAZ) and unaffected glass, and polymer delamination are circled

Figure 5.23 shows that the interface between the HAZ and unaffected glass had cracked in some of the TPVs drilled with CO_2 laser. Furthermore, there was slight delamination visible between the polymer laminate and the glass at the exit and entry side of the CO_2 laser-drilled TPVs. Since the cracking at the HAZ interface might have been a defect related to grinding and

polishing, an ion-milled sample was also prepared to confirm the cracking as shown in Figure 5.24.

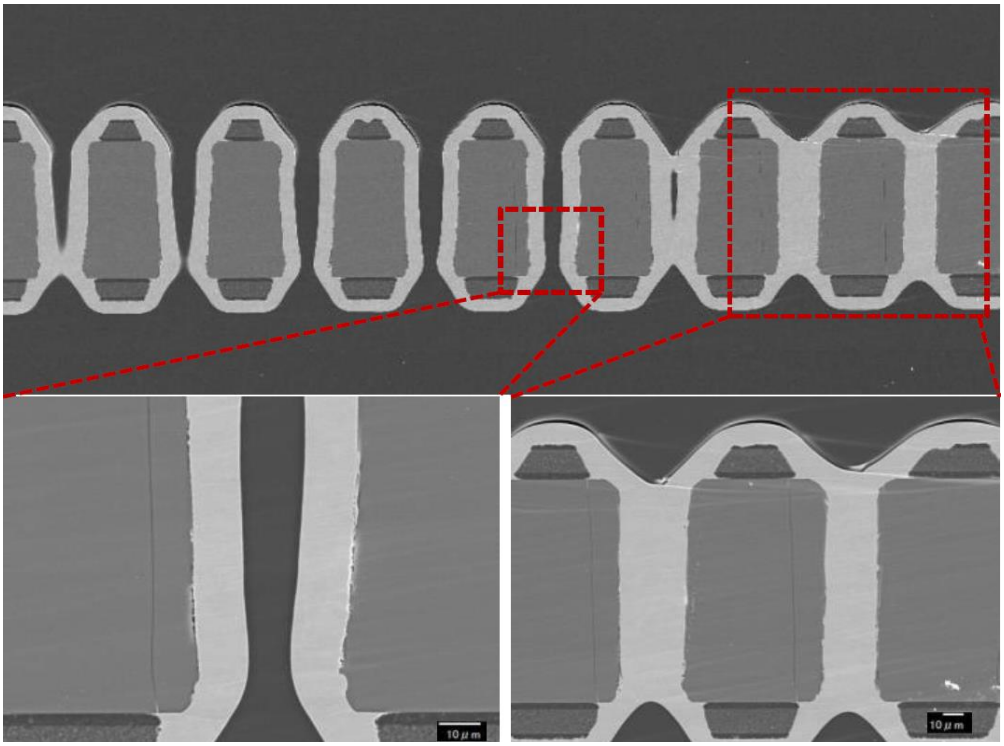


Figure 5.24. An ion-milled cross-section of a TPV array fabricated with the CO_2 laser, confirming the cracking at the interface between heat-affected zone (HAZ) and unaffected glass (Courtesy of NGK).

Fabricated structures were preconditioned according to moisture sensitivity level-3 (MSL-3) standards (60 ^{o}C, 60 % R.H. for 40 hours), followed by 3 times reflow at 260 ^{o}C peak temperature in order to investigate the effects of moisture absorption during lead-free board assembly processes. Fabricated structures were then placed into a thermal shock chamber to cycle between -55 ^{o}C and 125 ^{o}C with a dwell time of 15 minutes at each temperature extreme. The failure criterion was set as 10 % increase in daisy-chain electrical resistance. Cross-sections of TPV holes fabricated with CO_2 laser were prepared by dicing glass substrates. Dicing the

substrates, instead of preparing cross-sections by molding, grinding, and polishing, enabled to image the sidewalls of the vias. Figure 5.25 presents SEM micrographs of the CO2 laser- drilled TPVs.

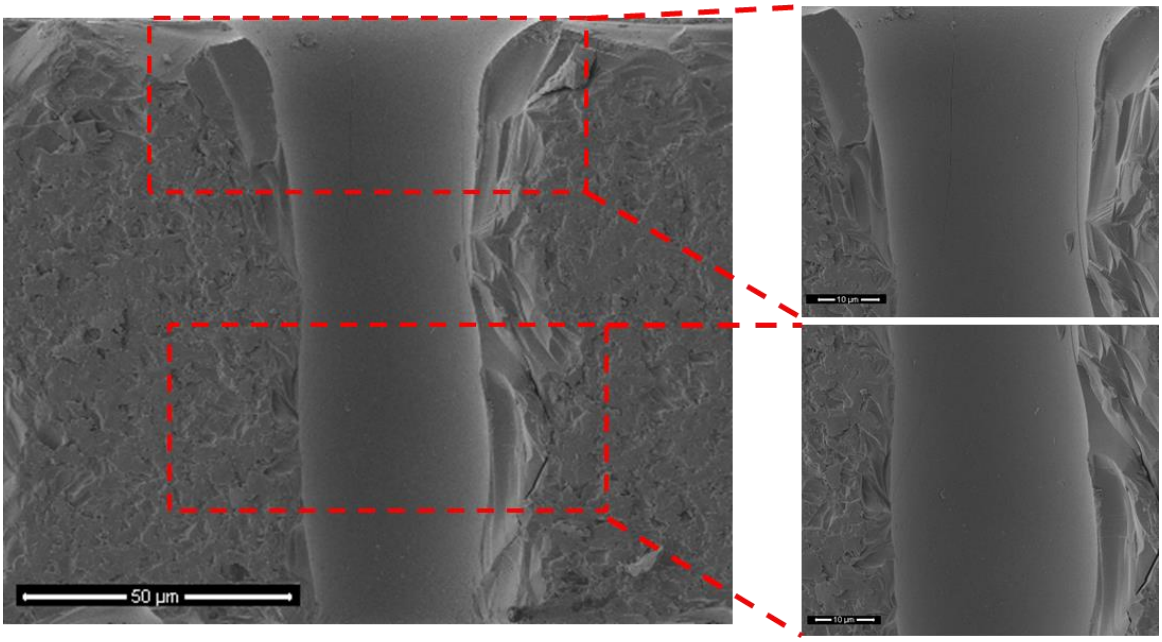


Figure 5.25. Cross-section SEM micrograph of a CO_2 laser-drilled TPV in bare glass. Vertical grooves are visible in the top right micrograph

TPV formation with the CO_2 laser, the via shape had funnel-like resemblance with curviness along the whole via. The entry and exit sites had no remarkable drilling debris accumulation. The sidewalls were smooth with minor debris, possibly from sample preparation. Furthermore, there were a few long grooves along the vertical direction of the TPV. The HAZ was not visible in the SEM micrographs. However, in the cross-section, the surfaces seem to have endured visible damage due to the dicing that might have obscured the HAZ. The via sidewall quality can affect the radio frequency characteristics of the interposer. Especially, high roughness in the sidewall can cause reflections or other distortions in propagating signals.

However, roughness in the sidewall may also provide mechanical anchoring of copper, resulting in better adhesion and thus may lead to increased reliability. This can become especially important in the case of fully-filled vias where copper extrusion is a known reliability risk in silicon interposers.

The CO_2 laser-drilled samples were tested for 1000 thermal cycles. The resistances of the daisy chains in the TCT coupons were measured several times during the test periods of 1000 cycles. The failure criterion was 10 % increase in the resistance of any via chain. Based on this failure criterion, no failures were observed in any of the test structures, drilled with CO_2 laser. Table 5.4 summarizes these results.

Table 5.4. Reliability Test of CO_2 laser-drilled TPVs in Glass

	CO_2	
Pitch	120 um	200 um
Array Size	10 x 10	10 x 10
Coupons	4	5
Via rows	40	50
Number of tested vias	290	420

Cross-sections were then prepared from both sample types and imaged via optical and electron microscopy to look for any visible changes compared to the as-fabricated samples as shown in Figure 5.26. The CO_2 laser-drilled samples did not display any marked differences compared to the as-fabricated samples either. The imaged samples had polymer delamination at the laser entry and exit-sides of the substrate in some of the vias. The delaminated-sample had

copper under the polymer, which indicated that the delamination had already existed during the metallization, rather than arising from the thermal cycling.

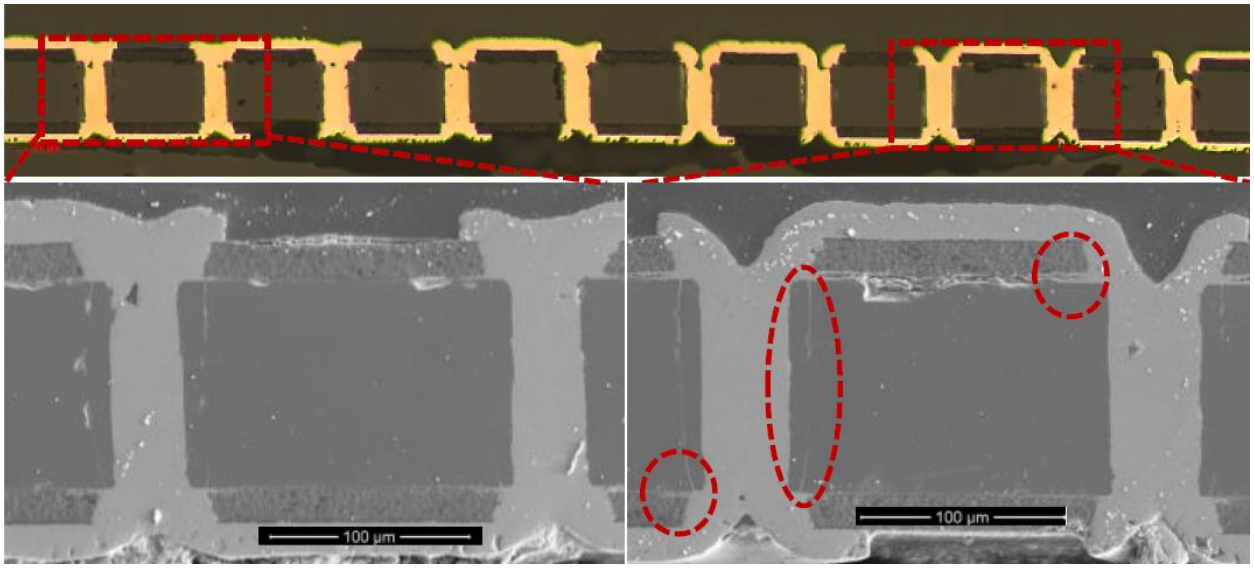


Figure 5.26. Optical and SEM micrographs of the CO_2 laser-drilled TPVs test vehicle after 1000 cycles

5.4 TPVs in Bare Glass formed by Laser-Assisted Chemical Etching

Following the bare glass interposer design guidelines and fabrication processes described in previous chapters, reliability test vehicles were designed, fabricated and subjected to reliability tests. These test samples consist of two metal-wiring layers and daisy-chain structures of TPVs, as shown in Figure 5.27. Each test coupon has 64 TPVs arranged in an 8x8 matrix. Each TPV chain is connected with a four-point Kelvin-Probe structure to enable sensitive resistance measurements without the influence of contact and wire resistances.

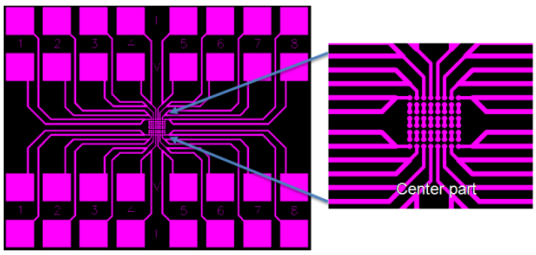
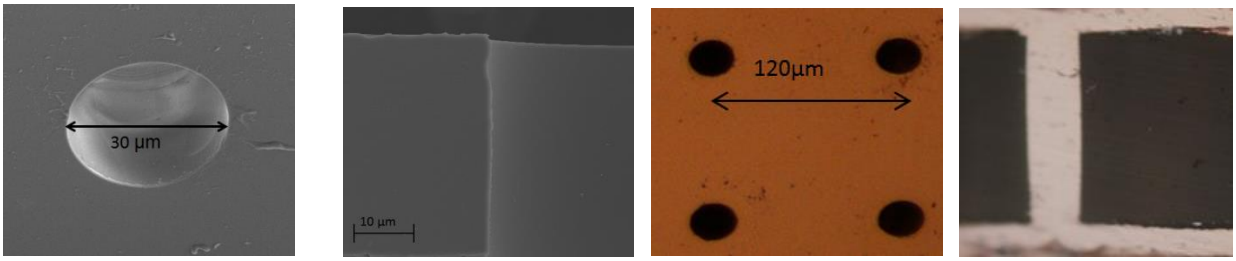


Figure 5.27. Layout of test vehicle and TPV daisy chains

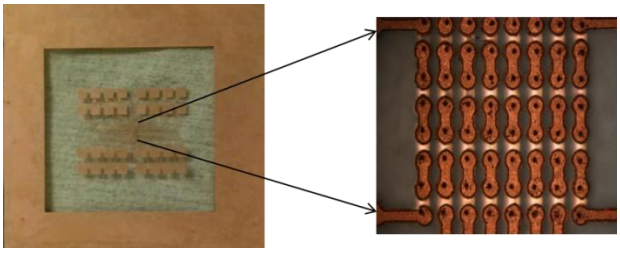
Bare glass panels with TPVs were provided by Corning Inc. Figure 5.28 shows the SEM images of 30 µm diameter TPV surface and side wall. It is seen that TPV side wall is smooth and free of microscopic defects that might act as stress concentrators initiating cracks in glass.



(a) (b) (c) (d)

Figure 5.28. (a) SEM images of via hole top view and (b) via sidewall, optical images of (c) top view TPV array at 120 µm pitch and (d) cross-section of TPV after metallization

Figure 5.29 shows the top surface image of the fabricated test vehicles.



(a) (b)

Figure 5.29. Fabricated (a) 2”x2” test sample with TPV chains and copper wiring used for reliability characterization

The test vehicles were first subjected to thermal cycling test as in JEDEC (JESD22-A104

condition B) test standards to evaluate the reliability of TPV. Three samples were tested consisting of a total of 192 TPVs. The samples were taken out at 250, 500, 750 and 1000 cycles, and every 1000 cycles thereafter up to 3000 cycles, and the daisy-chain resistances were measured to detect TPV failures. Distribution of resistance was attributed to varying copper thickness within samples. A resistance change of more than 10% of initial resistance was chosen as the failure criterion. All the TPV daisy chains survived 3000 thermal shock cycles with a stable resistance, confirming the thermomechanical reliability of TPVs in bare glass panels. No significant resistance changes were observed during the tests as illustrated in Figure 5.30. Small increments in daisy chain resistance were attributed to the oxidation of the unpassivated copper after exposure to the ambient air condition of the thermal cycling chamber.

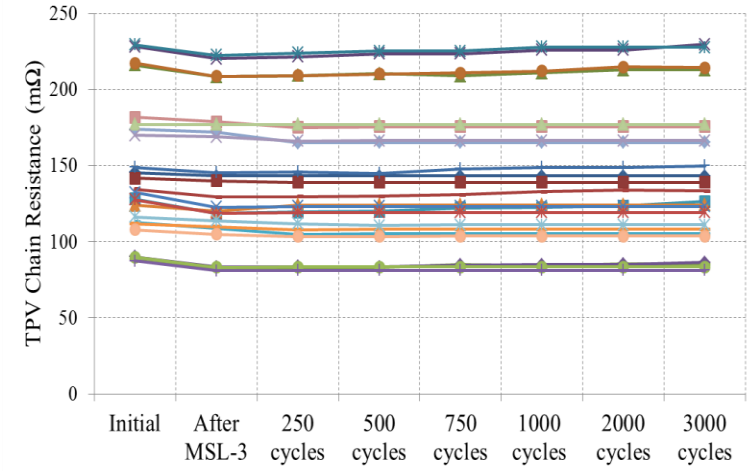


Figure 5.30. Distribution of TPV chain resistance and its variation during thermal cycling test

In order to characterize the reliability of TPV after thermal cycling test, SEM cross-sectional analysis was performed on the test samples. The samples were molded in epoxy resins to protect the glass samples and thus avoid any artificial cracking during cross sectioning. The

molded samples were fine-polished to expose the TPVs. No copper cracks were found even near the corners where larger plastic deformation occurs, which explains the approximately stable resistances during thermal cycling test. Consistent with the model predictions of high fatigue life of TPV, there was no Cu via failures after cycling for 3000 cycles. Plating defects such as voids and copper micro cracks due to stress concentration around voids were observed in certain locations as shown in Figure 5.31; however, they did not impact the electrical reliability.

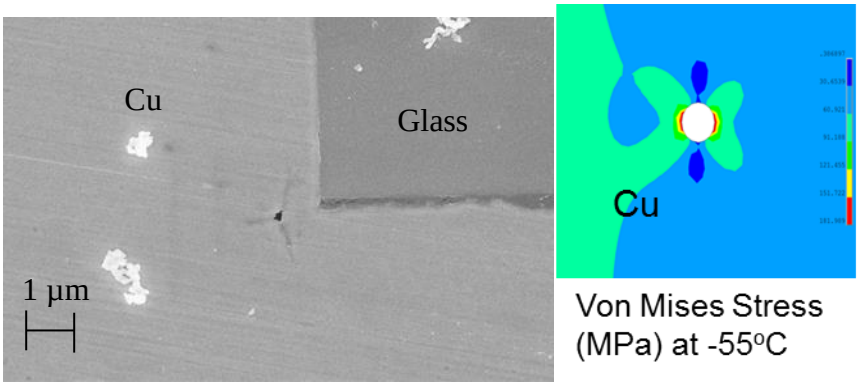


Figure 5.31. Micro cracks in copper due to stress-concentration from plating voids

Multiple images were captured at different locations to detect interfacial delamination and cracks in glass. Figure 5.32 shows Cu-glass interfacial separation under the Cu traces. This delamination was caused by the local high shear stress near the Cu trace outer edge, as predicted by modeling. Weak adhesion strength of copper to bare glass surface further increased the chance for delamination. Delamination did not continue through the TPV wall, presumably from the increased adhesion due to higher roughness on TPV sidewall compared to that on glass surface, and low radial peeling stresses due to conformal-plated TPVs.

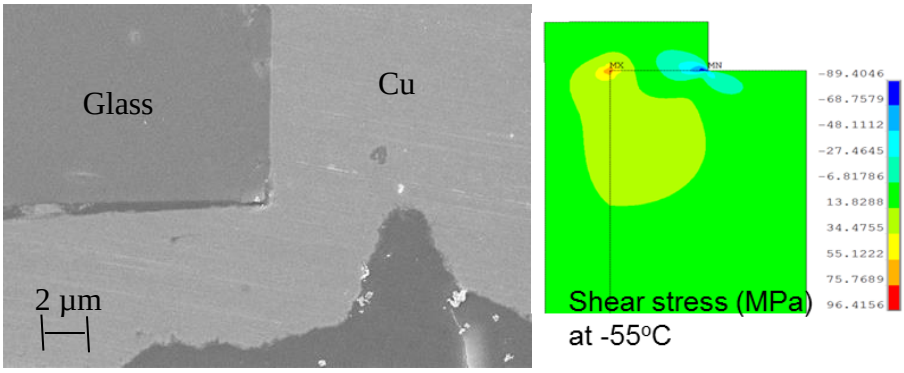


Figure 5.32. Copper delamination from glass surface near TPV corner

Figure 5.33 shows a crack that occurred around TPV corner where 1st principal stress in glass reaches its maximum value. Although these failures did not affect the resistance under current design and test conditions, they may result in negative impacts on the performance of TPVs. These failure points correspond to the localized high tensile stresses around TPV corner, leading to crack formation. Cracks were observed to localize around high-stress regions where the energy release factors are presumably high.

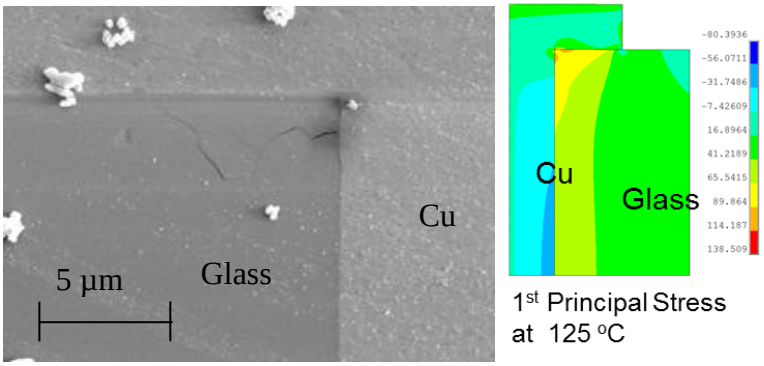


Figure 5.33. Crack in glass around TPV corner

Figure 5.34 shows copper-glass interface along TPV sidewall far below the surface. No delamination or glass-cracking failures occurred. This is due to significantly lower stresses in

this region away from TPV ends, as predicted by modeling results.

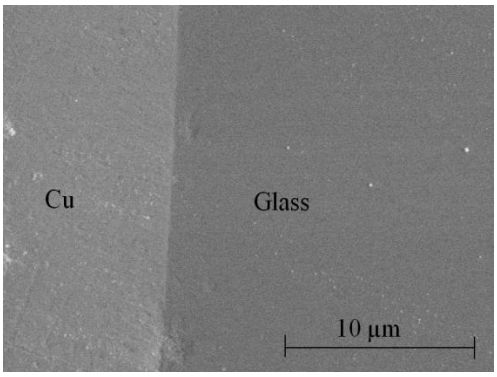
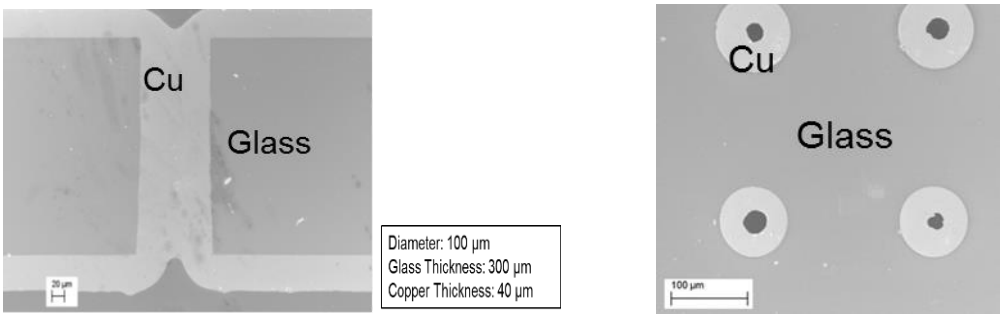


Figure 5.34.SEM image of Cu/glass interface far below surface

Secondly, similar test vehicle with higher copper thickness on thicker glass was fabricated. Aspect ratio was chosen as 3 ,and a conformal 40 µm copper was plated in 100 µm TPV diameter. As the radius ratio is increased, higher thermomechanical stresses were expected compared to the former sample. Thickness of titanium adhesion layer was increased for higher adhesion of copper to glass. Therefore, copper delamination failure was prevented. Also as expected there were no radial cracks as shown in Figure 5.35.



(a) (b)

Figure 5.35. (a) Cross-section of TPV with thick copper and (b) no radial cracks after thermal cycling

Cross-sectional analysis after thermal cycling revealed a glass cracking failure mode as shown in Figure 5.36.As expected from modelling, there is stress singularity at the edge of TPV

pad. This localized high stress can lead to delamination of copper or cracking in glass due to glass cratering mechanism as described in [82]. Due to high adhesion of copper in this case, delamination did not occur. Instead the stress concentration at TPV pad edge led to cracks in glass arching to the other stress concentration at TPV corner. The magnitude of stress at TPV pad edge is dependent on the diameter of the TPV pad. Diameter of landing pad can be decreased to reduce probability of glass cratering. Two avoid both copper delamination and glass cracking, glass surface should be laminated with a thin polymer which is described in next part.

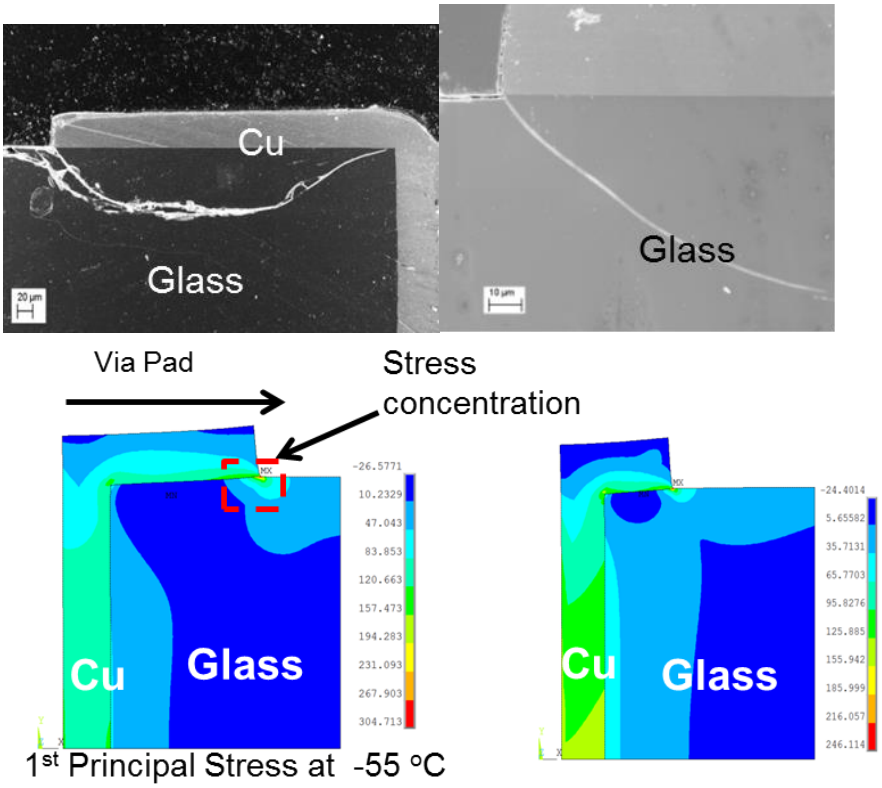


Figure 5.36. Cracks in glass initiating from TPV landing pad and reaching to TPV corner where high stress concentrations are expected from modelling.

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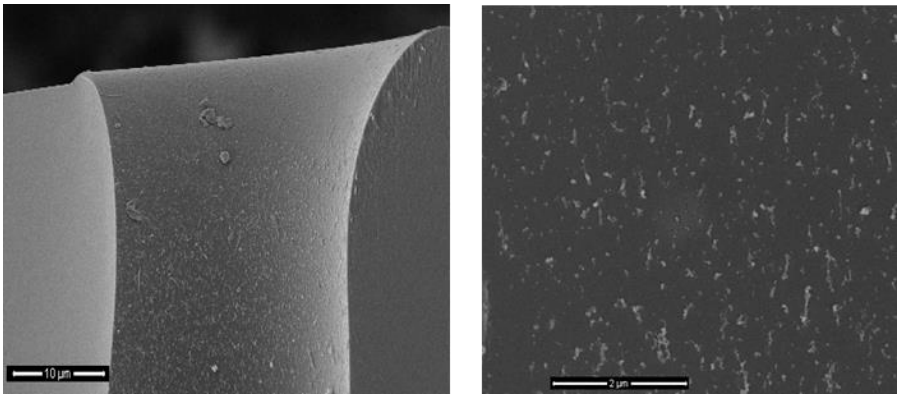
5.5 Thin-polymer laminated glass with Via-First TPVs formed by Electrical Discharge

Following the processes described in Chapter 4, test samples were fabricated to evaluate the thermomechanical reliability of TPVs in glass panels. Via formation by electrical discharge method is not compatible with polymer-laminated glass. Therefore, vias were formed by electrical discharge process on 6" bare glass panels of 100 µm thickness from Asahi Glass Co. Via formation occurs by focusing a controlled electrical discharge current to create locally molten region of glass, followed by dielectric breakdown and removal of glass. With this process, via diameters of 20 µm at 50 µm pitch was achieved. For reliability test samples in this study, through-vias with 60 µm entrance diameter and 220 µm pitch were used. SEM image of TPV cross-section before fabrication process is shown in Figure 5.37. Curvature at via entrance was observed. TPV wall was free of defects and cracks that can act as stress concentrators. In via sidewalls, roughness in range of few nanometers was observed that can provide adhesion by mechanical anchoring of electroless copper onto bare glass.



(a) **(b)**

Figure 5.37. SEM images of (a) TPV entrance, (b) TPV wall

Figure 5.38 shows defects formed during TPV formation in entrance of some TPVs where high stresses are expected during thermal cycling. However, defect size is lower than 2µm, which is considered safe for conformal plated TPVs from modeling.

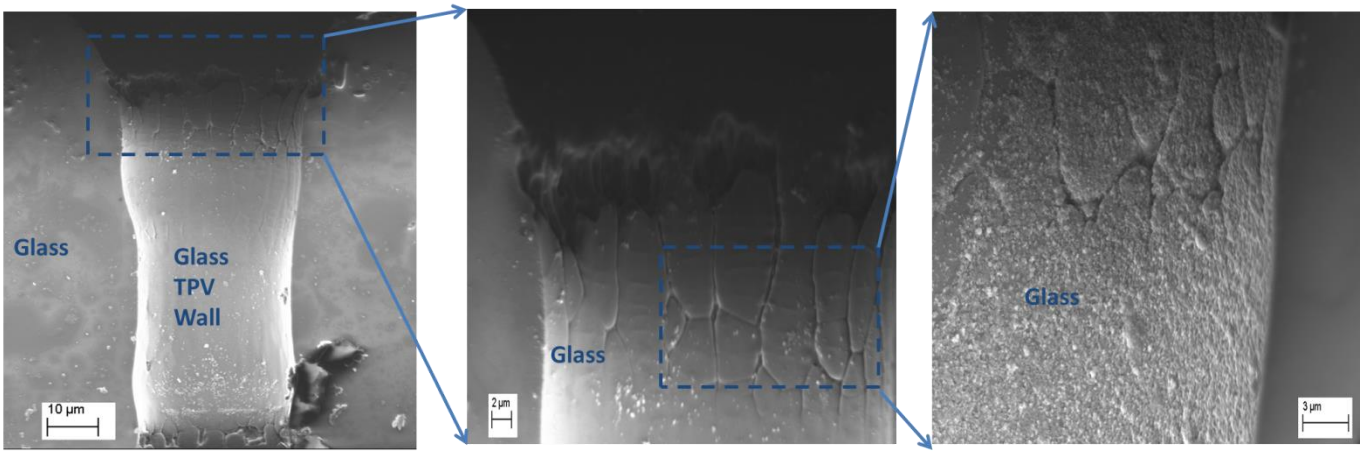
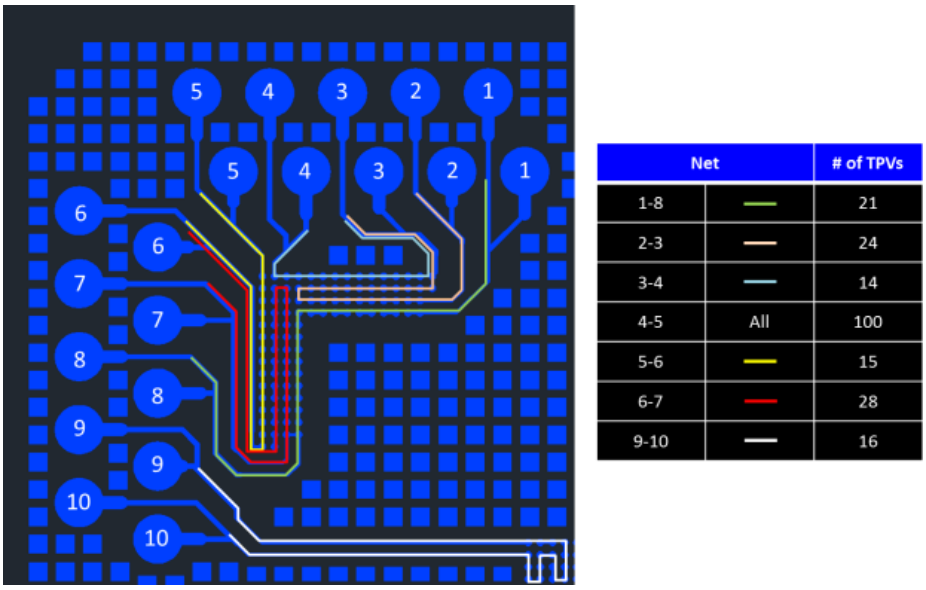


Figure 5.38. SEM cross-section of TPVs formed by electrical discharge process

The test vehicles consisted of two metal wiring layers and varying number of TPV transitions that form daisy chain structures. At the ends of each daisy chain, four-point probe pads (Kelvin structures) were included to enable sensitive resistance measurements by correcting for the influence of contact and wire resistances. Test samples were designed with TPVs of 60 µm diameter at 220 µm pitch. Layout of the test sample is shown in Figure 5.39. Dummy metal squares are added in order to have uniform current density throughout the sample, resulting in approximately same electroplated copper thickness.



(a) **(b)**

Figure.5.39. (a) Layout of test samples with TPVs, wiring and Kelvin probe pads (b) Daisy chains with varying number of TPV transitions

After fabrication, 5 test coupons with a total of 1000 TPVs were diced from the same 6" glass panel, which resulted in 10 daisy chains, each with varying number of TPVs, as illustrated in Figure 5.40. Before proceeding to thermal cycling, initial resistances of each chain were measured. Average values of these measurements are shown in Figure 5.30. Linear growth in resistance with the number of TPVs was observed since the diameter and pitch of TPVs was same throughout the panel, leading to a directly proportional increase in length. Addition of each TPV to the daisy chain increased the resistance by approximately 15 mΩ.

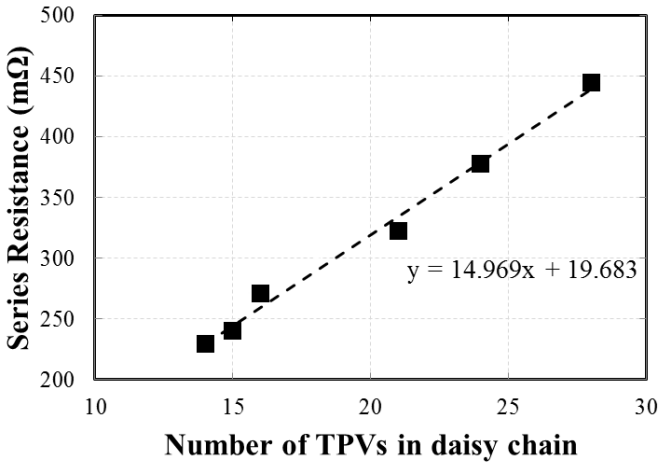


Figure 5.40. Initial resistances of daisy chains with different number of TPV transitions.

Test samples were placed in a Thermotron 7800 oven and cycled from -55^{o}C to 125 ^{o}C by dwelling at each temperature extreme for 15 minutes. The samples were taken out of the chamber after completing 250, 500, 1000 and every 1000 cycles thereafter, up to 3000 cycles. The resistances of the daisy chains were measured with a four-point probe to detect failure initiation in copper TPVs. A resistance change of more than 10% of initial resistance was chosen as the failure criterion. No significant resistance changes were observed in daisy chains during the tests as illustrated for daisy chain of 100 TPVs in Figure 5.41.

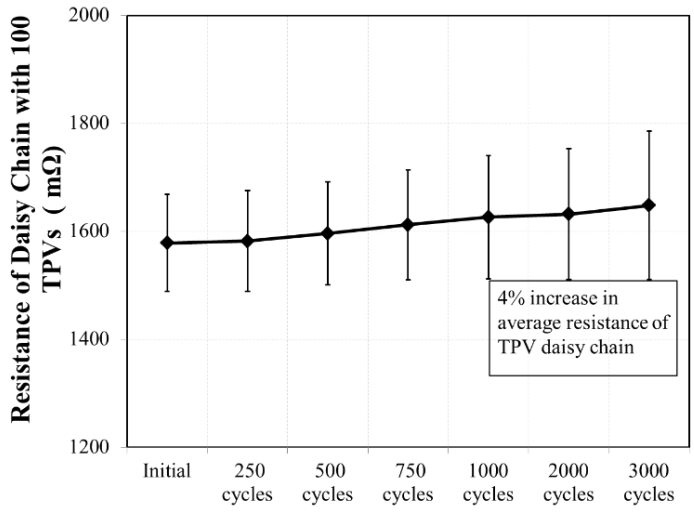


Figure 5.41. Average resistances during thermal cycle testing of 10 daisy chain structures with 100 TPVs. Error bars represent the standard deviation.

Based on the chosen failure criterion, all TPV daisy chains survived 3000 thermal shock cycles, confirming the thermomechanical reliability of TPVs fabricated with this via-first process in bare glass panels. Small increments in daisy chain resistance were attributed to the oxidation of copper surfaces inside thermal cycling chamber. To characterize the samples after thermal cycling tests, test samples were molded in epoxy resins, cross-sectioned and then fine-polished to reveal TPV structures. Figure 5.42 shows the optical cross-section image of daisy chain after thermal cycling. The electrical discharge TPVs did not show any visual deviation from the as-fabricated samples before thermal cycling.

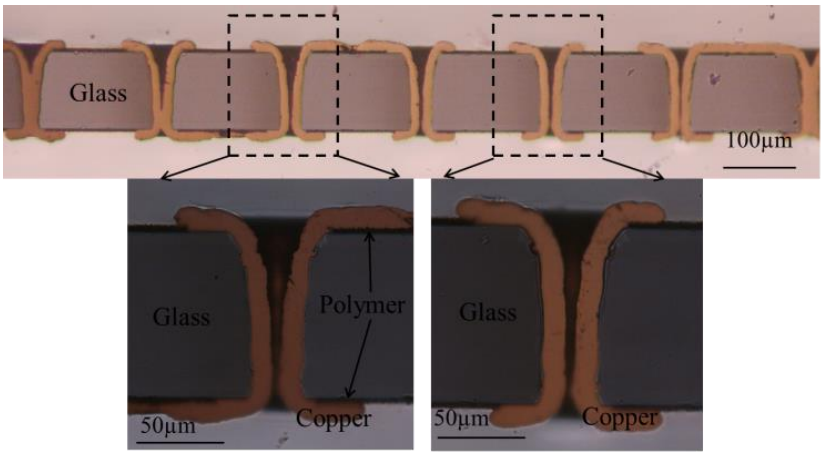
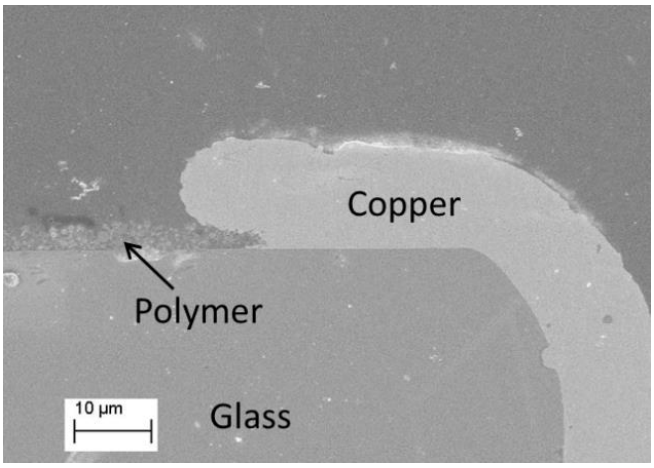
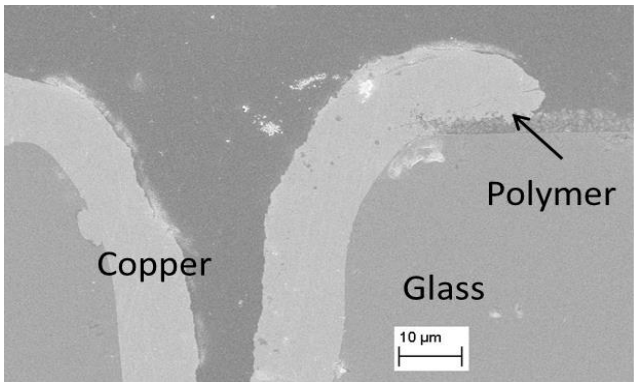


Figure 5.42. Optical image of TPV test structures after thermal cycling

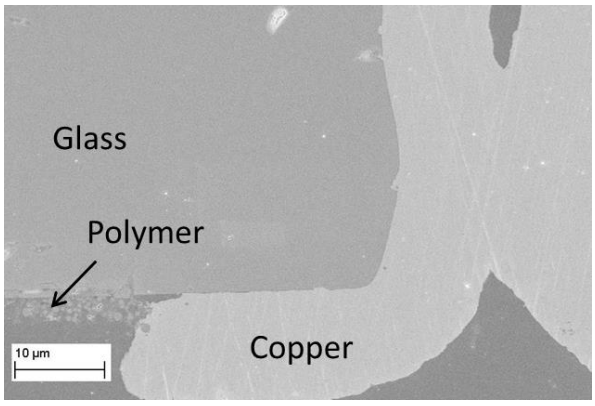
SEM images were taken at different locations in TPV. No copper cracking was found, which explains the absence of any significant changes in daisy chain resistances. Furthermore, no glass cracking was observed, which can be attributed to reduced principal stresses in glass due to stress-buffering of polymer and smooth curvature at corners with via-first process rather than the sharp via corners seen with other laser-via formation processes. The highest stresses in glass are reduced by 50%, from 120 MPa with bare glass to ~60 MPa with the introduction of polymer films between copper and glass. Magnified images at entry and exit sites were captured to analyze the interfaces between different materials, where shear stress localization occurs. As seen in Figure 5.43, there were no delamination failures that can be attributed to adhesion of copper to thin polymer.



(a)



(b)

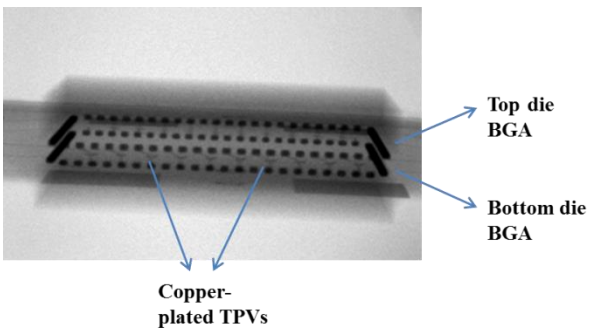


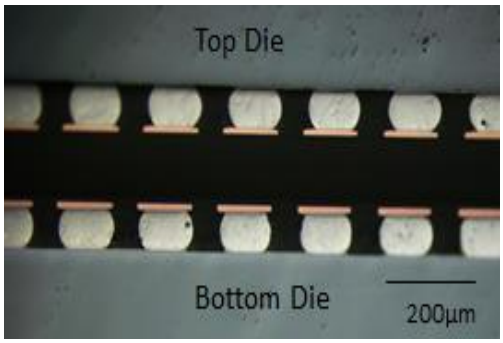
(c)

Figure 5.43. SEM images of TPV (a) entrance, (b) entrance and (c) exit sides. No cracking of glass or copper delamination was observed.

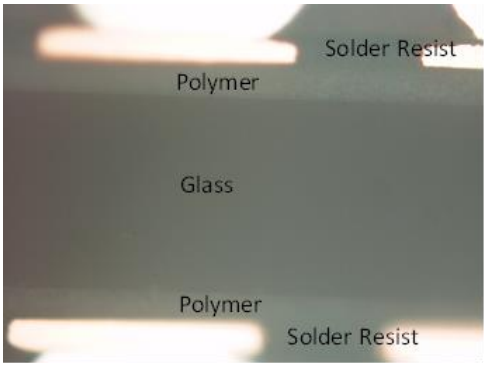
5.6 TPVs after 3D Assembly

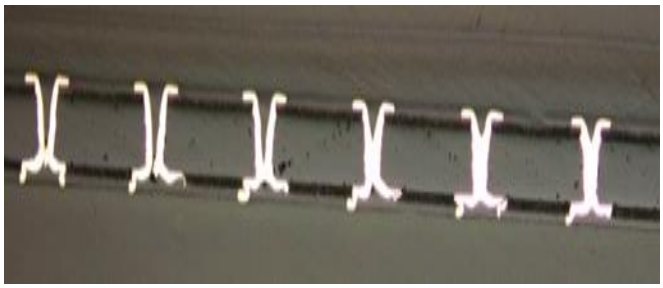
The reliability of UV laser-drilled TPVs were characterized using glass interposer test vehicles with double-side assembly. Following the fabrication processes described in Chapter 4, test vehicles are designed to form daisy chains consisting of TPVs in glass and solder bumps belonging to ICs assembled on both sides of interposer. When any interconnect in this chain fails, the whole daisy-chain fails. This type of design enables to test reliability of both solder bumps and TPV simultaneously. A commercial flip-chip daisy-chain test die was used for fabricating the test vehicles (PBO8) that has 22 solder bumps on each side. In each test coupon, there are in total 20 TPVs that connect the top and bottom dies. As a result, a whole daisy-chain is made up of 22 solder bumps, 10 TPVs and redistribution layers between them. After fabricating the 6”x6” glass interposer, it was singulated into 12mm x 12mm individual coupons by mechanical dicing. Distance between TPVs and bump pads in each test coupon was varied in order to assess the effect of interactions between them as shown in Figure 5.44. Flip-chip test dies were sequentially assembled on both sides of glass coupons by solder reflow followed by applying underfill. Test dies were connected through TPV chains in a way to enable reliability testing of the entire package. Figure 5.44 summarizes the structure of the test vehicle.





(a) **(b)**





(c) **(d)**

Figure 5.44. (a) X-ray image of interposer after IC assembly, (b) Cross-section of test vehicle with double-side assembly, (c) sample stack-up and (d) TPV array connecting the top and bottom ICs.

The fabricated test vehicles were then subjected to accelerate liquid-to-liquid thermal cycling test between -55°C and 125°C with a dwell-time of 5 minutes at each temperature extreme. In total, eight test coupons were tested. Along with assembled test coupons, chains of 10 TPVs in 4 free-standing glass coupons were subjected to accelerated reliability test in order to observe the effect of die assembly on TPV reliability. Test results are summarized in Table 5.

Table 5.5. Reliability test Results for TPVs in 3D Package

Test Coupon	Total # of coupons	Total # of TPVs	Pass/ Fail
TPV chain in free-standing glass	4	40	4/4
Assembled test vehicle with dies	4	80	4/4

Electrical resistances of the TPV-solder bump daisy-chains were monitored periodically to identify the initiation of cycling-induced failures. Resistance of the whole chain varied between 0.8 - 1Ω and did not change by more than 10% up to 1000 thermal cycles. The reliability characterization results with 3D interposer samples did not show any failures up to 1000 cycles, as predicted by the models. A daisy chain that passed reliability test is shown in Fig.19. However, after further thermal cycling up to 2000 thermal cycles, resistance increase was observed on majority of chains. The samples were characterized using optical cross-section images to investigate the failure locations and mechanisms. The failures were mainly attributed to solder bump cracks, with a majority found around the bump-die interfaces. These are summarized in Figure 5.45.

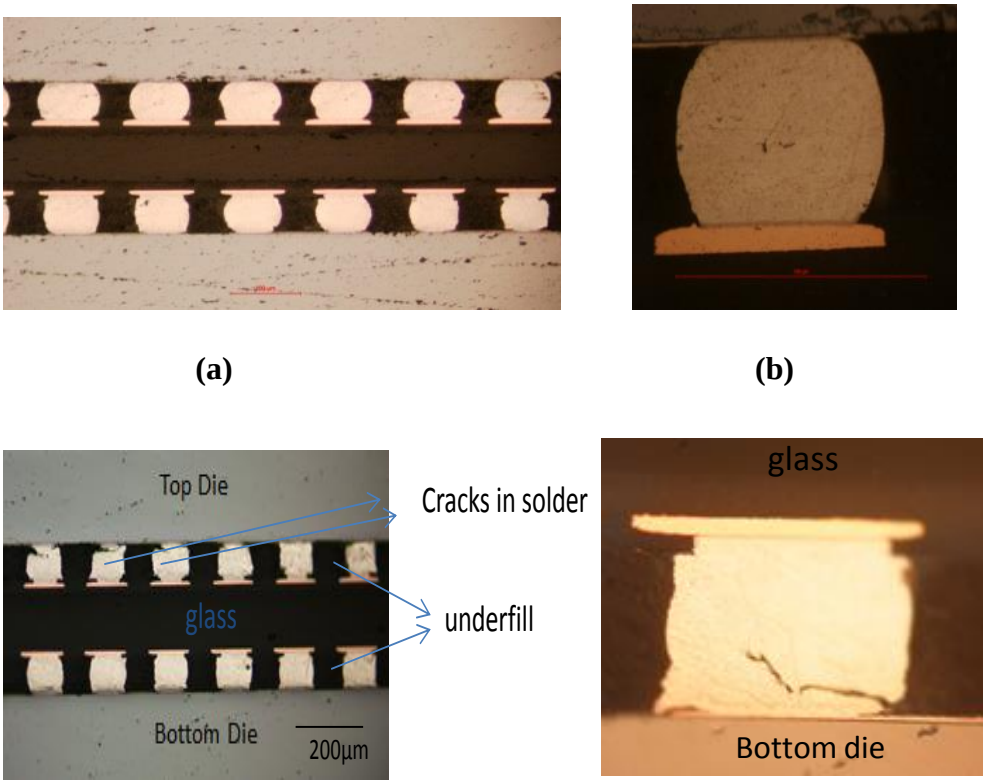
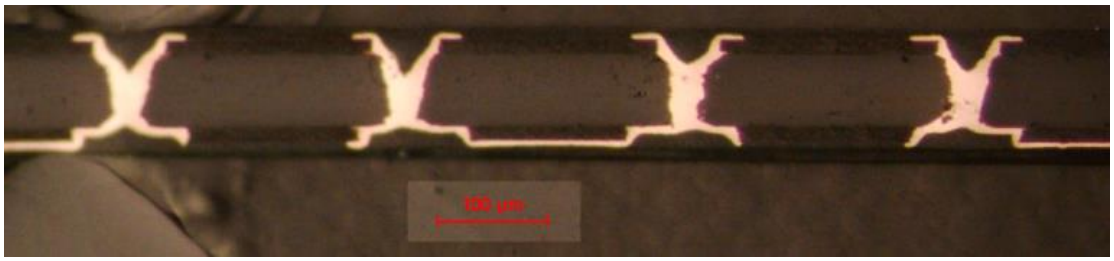
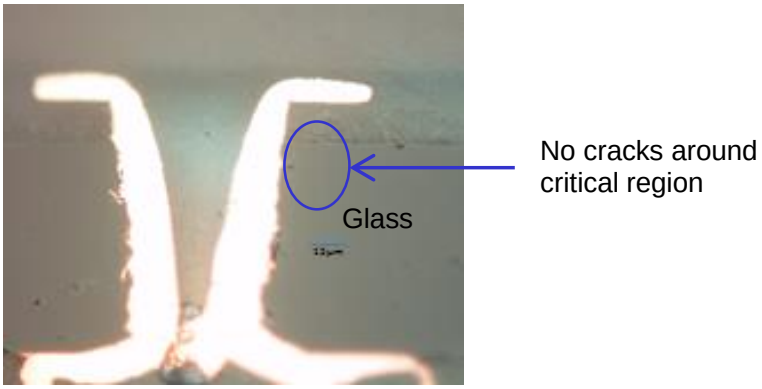


Figure 5.45. (a) Cross-section of a passed saple, (b) Passed Solder bump, (c) cross-section of a failed sample after thermal cycle test.and (d) Failure in solder ball after thermal cycle.

There were no failures related to TPV and glass interposer in the form of major cracking around high-stress regions. An array of TPV daisy-chain after 2000 cycles is shown in Figure 5.46. Thermal cycling did not lead to any growth of defects in TPV arrays both in free-standing glass and double-side assembled configuration as expected from mechanical modeling. As predicted by FEM, TPV in 3D assembly experienced similar stresses as in free-standing glass. Therefore, electrical failures first initiated in solder bump which were detected by resistance measurements.



(a)



(b)

Figure 5.46. (a)Cross-section of TPV after thermal cycling test and (b) TPV after thermal cycling test

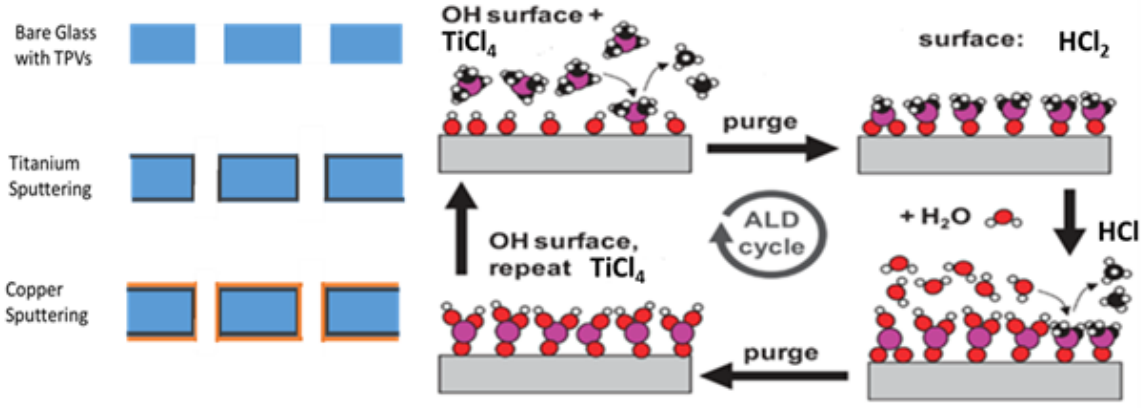
5.7 Raman Characterization

In the previous chapters, finite element modeling- based TPV design guidelines for lowering these thermo-mechanical stresses were presented and reliability of TPVs was experimentally demonstrated. FEM techniques, however, often provide qualitative trends in stresses and strains because of the lack of accurate thermo-mechanical properties of TPV materials leading to significant discrepancy between the modeled and fabricated structures. Direct stress measurement is a powerful method to validate the models and to refine the material properties accordingly. Such measurements are also effective in providing direct correlation between materials, geometries and reliability performance. Raman spectroscopy is an effective

technique to verify mechanical modeling- based guidelines and quantify stresses in glass in the vicinity of copper-plated TPVs. These measurements provide valuable guidelines for design and material selection. When a material is illuminated with monochromatic light, photons can interact with lattice vibrations (phonons) of the material. Due to this interaction, which is called Raman scattering, phonons in the material can be excited to a higher energy level or dropped to a lower energy level [90]. The first is called Stokes Raman scattering, the second Anti-Stokes Raman scattering. Thus, the scattered light contains different frequency components than the incident light. The spectrum of the scattered light contains frequency components with a certain frequency higher or lower than the frequency of the incident laser light, which can be detected.

So, from the spectrum, one is able to know the characteristic frequency of the material vibrations. Shifting of photons to a higher energy level is the most common process to occur and Raman spectroscopy concentrates on detecting peaks associated to that process. As a result, the spectrum of scattered light contains information about characteristic frequencies of material vibrations. This spectrum can be altered when material is under stress that forms the basis for piezospectroscopy. Piezospectroscopic effect is defined as the shift in the frequency of a spectroscopic transition in a solid in response to applied strain or stress. Thus, by measuring the shift in the spectra, the lattice strain can be determined. Compressive stress (σ negative) results in an upward shift of the Raman peak, while tensile stress (σ positive) results in a downward shift. The relation between Raman shift and strain is calculated by secular equation depending on phonon deformation potentials. Eigen values give the difference between the Raman wavenumber of each mode in the presence of stress and absence of stress. If uniaxial or biaxial stress is present in the sample, this secular equation is simplified.

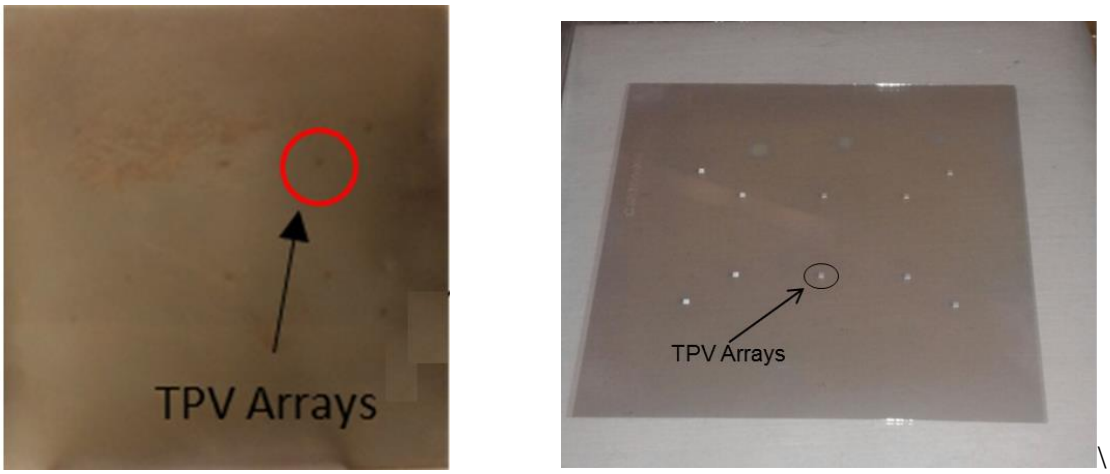
In literature, Raman spectroscopy has been used to quantify stresses in silicon around Through-Silicon-vias (TSVs) [91,92]. High signal-to-noise ratio of Raman signals obtained from silicon, and availability of various formulae that relate stress in silicon to peak shifts, enabled Raman stress analysis in TSVs. However, luminescence property of glass and its amorphous structure presents challenges in Raman analysis of TPVs in glass interposers. This challenge is addressed with recent identification of shift in Raman scattering peaks in copper oxide and Titanium oxide [93]. When a thin film of copper on glass is oxidized, its ductility decreases those results in better transfer of glass stress to the thin copper oxide film. Therefore, thin film of copper oxide is approximately in the same stress state as the glass surface and can be utilized as a stress sensor. Raman active titanium oxide films can also be deposited on glass [94]. Monitoring the stress of these films on glass using Raman spectroscopy can possibly give information about stress in glass. In order to assess the effect of mechanical stress on Raman spectrum of copper oxide and titanium oxide, glass samples with TPVs were fabricated following the steps shown in Figure 5.47.



(a) **(b)**

Figure 5.47. Fabrication process for glass with (a) copper oxide thin film and (b) titania

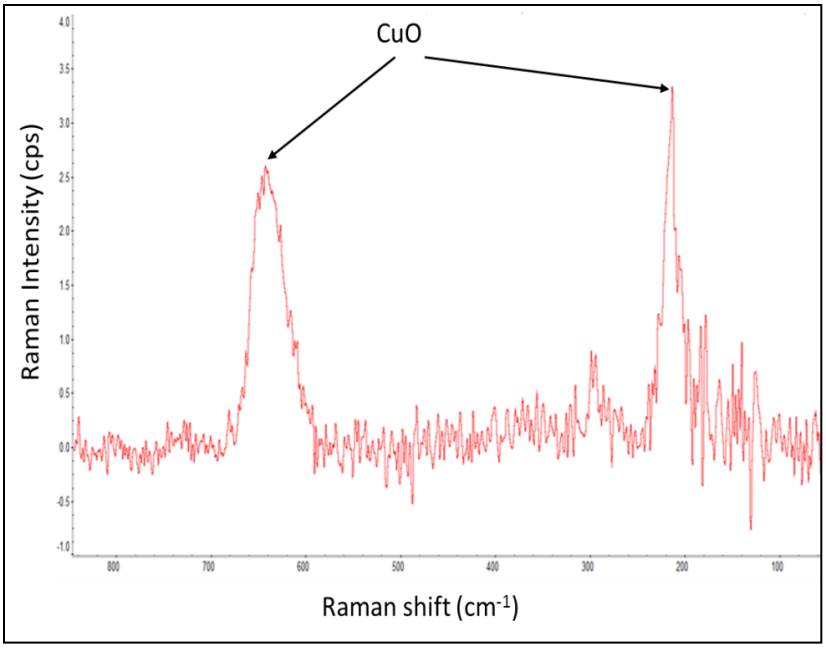
Glass panels (3”x3”) were metallized by Ti/Cu sputtering. The thicknesses of glass was 237 µm, and TPV diameters was 60 µm. TPV formation is achieved by chemical-assisted laser drilling process. Ti/Cu sputtering is applied on 237 µm thick glass with 60 µm TPVs. For oxidation of the copper, samples were annealed at 250^{o}C in air for 60 minutes. Titanium oxide (Titania) is directly deposited in anatase form by atomic layer deposition on 137 µm thick glass with 30 µm TPVs. The fabricated test samples are shown in Figure 5.48.



(a) **(b)**

Figure 5.48. (a) Bare glass with copper oxide and (b) bare glass with anatase titania

Figure 5.49 shows Raman spectrum of CuO, and peaks around 160-230 cm^{-1} and 620-660 cm^{-1} ranges along with Titania with a stress sensitive anatase peak around 144-150 cm^{-1} and 400-410 cm^{-1}. These wavenumbers are close to the values reported in the literature confirming the calibration of Raman spectrometer used in the study. In this study, focus is on the stress sensitive peaks that appear in the range 620-660 cm^{-1} for copper oxide and 144-150 cm^{-1} for anatase.



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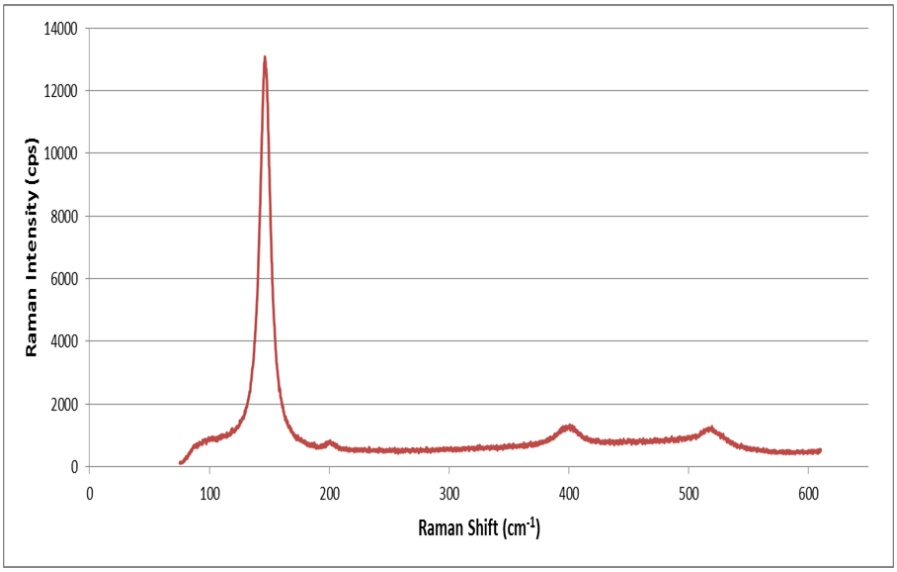


(b)

Figure 5.49. Raman spectrum of (a) Copper oxide and (b) anatase Titania

Next, the glass samples are subjected to mechanical bending to a certain radius of curvature as illustrated in Figure 5.50. The tensile stress on top glass surface can be assumed uniaxial and transferred to the deposited thin film of copper oxide or Titania. This tensile stress

is given as $\sigma = \frac{e\,E}{2\,R}$ where e, E and R are glass thickness, Young's modulus and radius of curvature respectively.

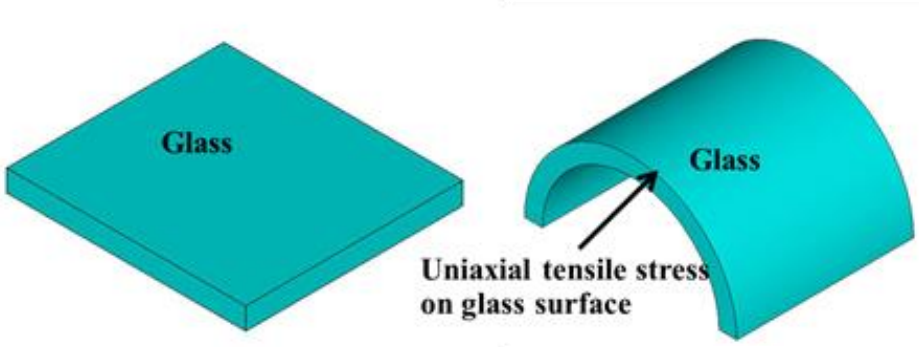


Figure 5.50. Mechanical bending of test samples creating a uniaxial tensile stress on the top surface.

Ti/Cu sputtered 3"x3" 237 μm glass was bent to a radius of 250 mm. Downwards shift was observed in CuO spectra due to uniaxial tension stress from bending, as shown in Figure 5.51. Using the stress formula, tension on copper oxide can be calculated approximately as 30 MPa, resulting in a shift of 5cm^{-1} in Raman spectra, which gives 6 MPa/ cm^{-1} piezo spectroscopic coefficient for Copper oxide thin films on glass. This is quite low value for a piezo spectroscopic coefficient; however it can be described by the wide peaks of copper oxide that are not very well defined.

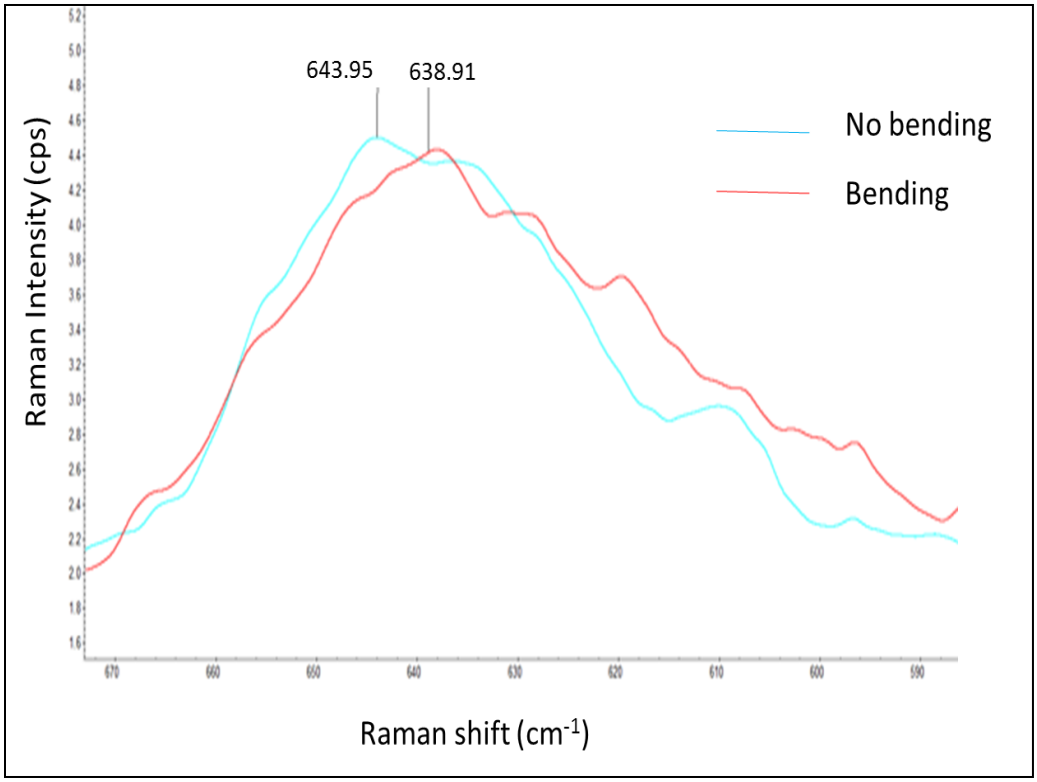
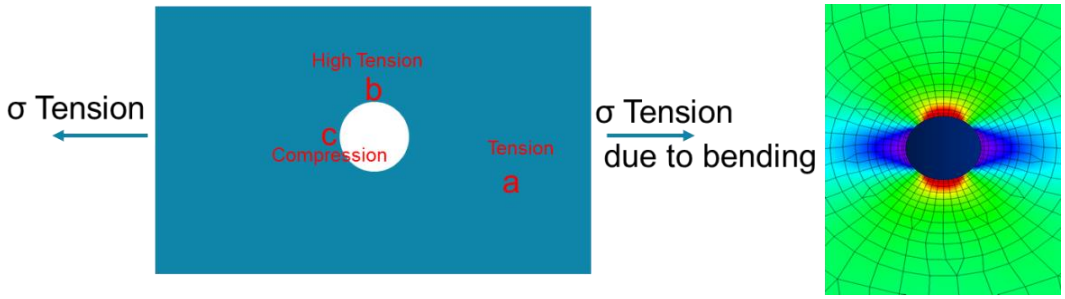


Figure 5.51. Shift in copper oxide spectrum due to bending

Anatase titania, deposited on 3"x3" glass with 137 µm thickness, was bent to a radius of 70 mm. When the sample is bent, uniform tension on the top surface gets modified around the via, as illustrated in Figure 5.48. Hoop stress (σ_b) at the top edge is approximately 3 times the tangential compression (σ_a) at the side edge (Figure 5.52). These stress relations are expressed as $\sigma_b \cong 3\ \sigma_a$ and $\sigma_c \cong -\ \sigma a$ [95]. Therefore, the glass around the TPV hole is subjected to uniaxial stresses, however with different magnitude and sign. As the TPV diameter is much smaller than the width of glass (3"), the diameter doesn't impact the stress magnitudes. These stresses are transferred to the titania film, which acts as the Raman-active stress sensor.



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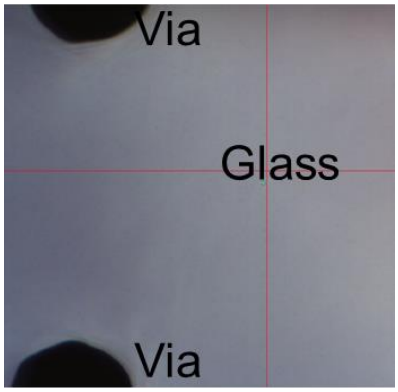


(b)

Figure 5.52. (a) Stress distribution in glass surface due to mechanical bending and (b) optical image of sample and points of measurement

At each point, 20 Raman spectra measurements were taken and averaged. Stress due to bending can be approximately calculated as 75 MPa. Average peak position before bending is 146.81cm^{-1}. Full width at half maximum is 10.5 cm^{-1} , which indicates that anatase shows a much sharper peak compared to copper oxide. The average peak positions at each point after bending are summarized in Table 6 and plotted in Figure 5.52. From this graph, piezocoefficient of Titania can be estimated as 1034 MPa/ cm^{-1} that shows 10% difference with values from literature (937 MPa/ cm^{-1}).

Table 5.6. Raman peak measurements averaged for different points on glass

Point	Average Peak position	Approximate Stress (MPa)	Peak shift from Initial state (cm^{-1})
A	146.73	75	-0.08
B	146.59	225	-0.22
C	146.88	-75	0.07

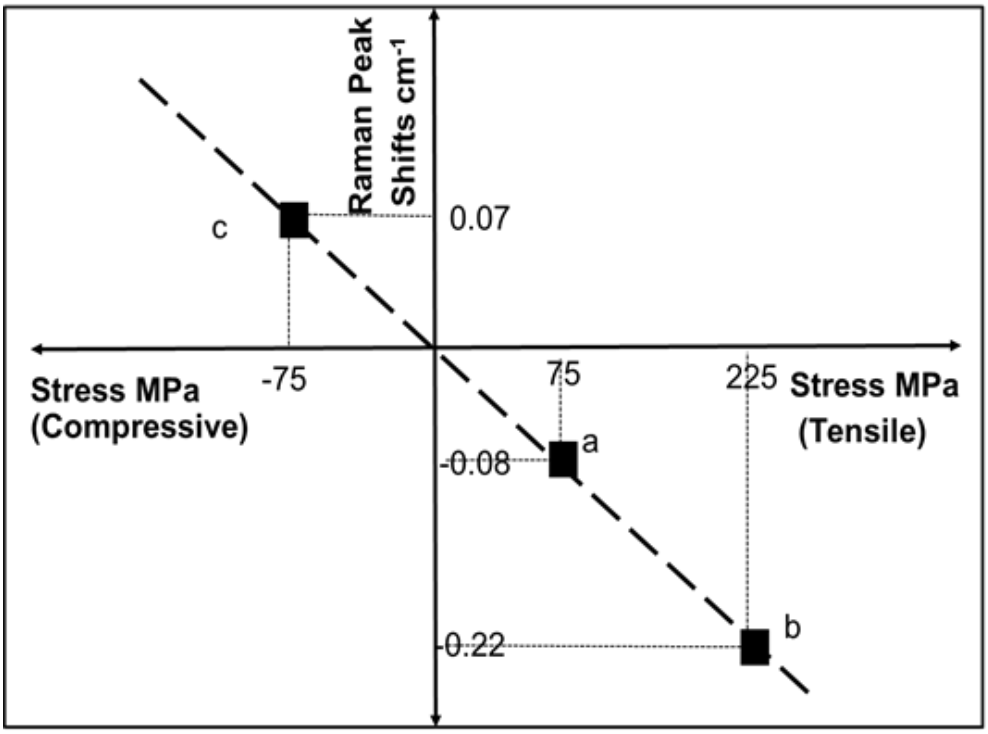
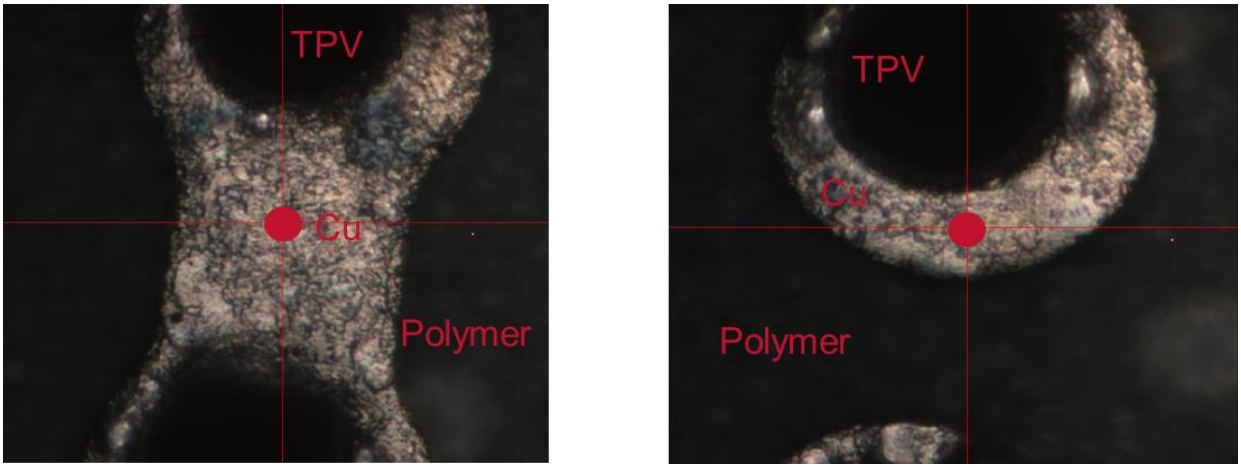


Figure 5.53. Uniaxial stress vs Raman peak shift for different points on glass

Next, using the same ALD process, copper-plated TPVs in polymer-laminated glass was coated with anatase Titania. The test samples were then heated to 150^{o}C to induce thermomechanical stresses in the vicinity of TPV due to the CTE mismatch between copper and glass. The impact of this thermomechanical stress on Raman spectra was investigated by taking measurements on points shown in Figure 5.54.

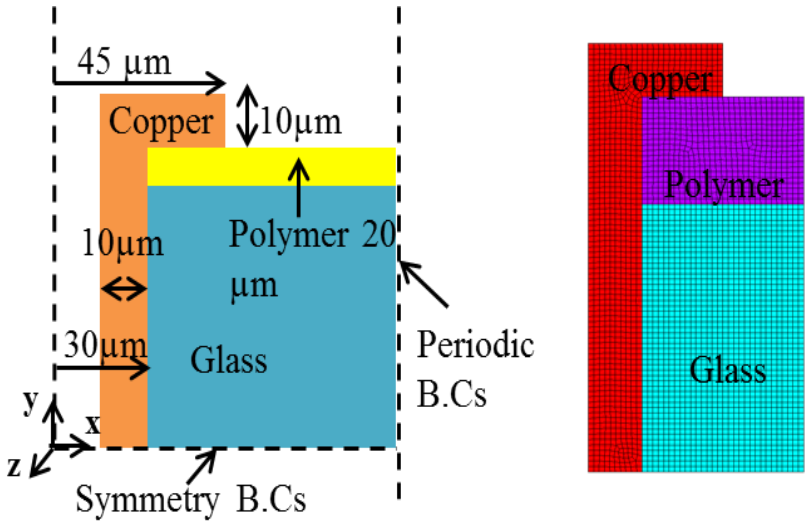


(a) **(b)**

Figure 5.54. Points of Raman spectra collection (a) in middle of TPVs where thermomechanical stresses are low and (b) in vicinity of TPV where stresses are high

Copper underneath the titania resulted in shift and widening of the anatase peak; in spite of this, the CTE-mismatch induced stresses at 150 ^{o}C can be resolved through piezospectroscopic measurements. At the center of the TPVs, peak location was measured to be 151.90 cm^{-1} , while in the vicinity of the TPV, the same peak was located at 151.85 cm^{-1}, indicating a peak-shift of 0.05 cm^{-1}. Using the piezospectroscopic coefficient of Titania as 1034 MPa/ cm^{-1}, the corresponding stress can be estimated as 52 MPa.

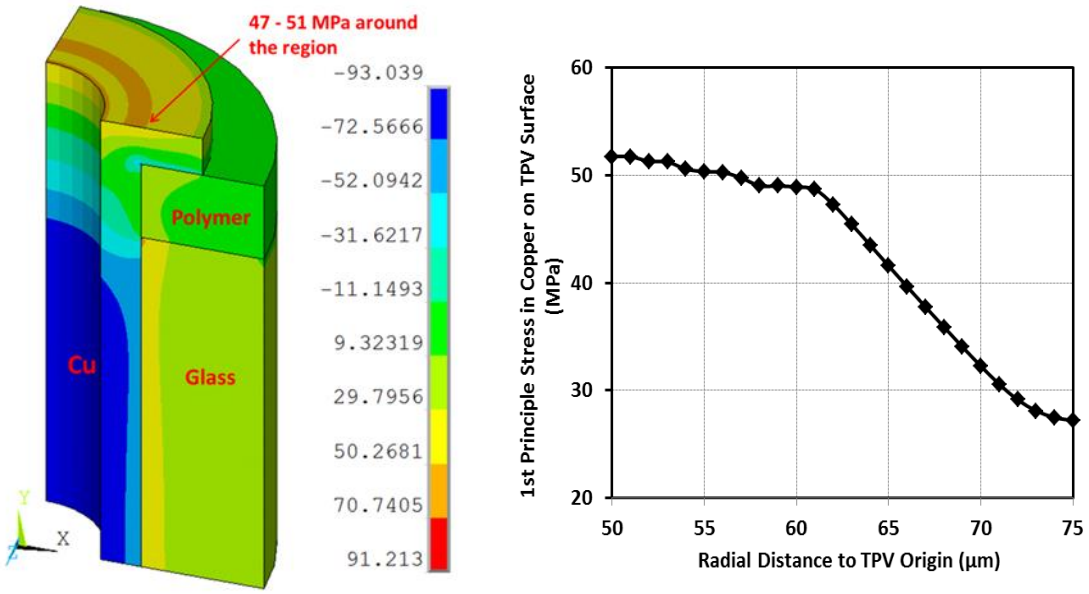
Finite Element modeling can be used to predict stress on top surface of TPV where the Raman spectra collections were conducted. A 2D axisymmetric model was built to analyze CTE mismatch stresses at 150^{o}C. Due to the symmetry of the structure, 1/4th TPV was modeled as shown in Figure 5.55 along with boundary conditions and dimensions.



(a) (b)

Figure 5.55. (a) Schematic of TPVs used for mechanical modeling and parametric analysis, (b) meshed 1/4th TV model

At high temperatures, expansion of copper creates radial compression and tangential tension in glass. On the other hand, at cold extremes, contraction of copper creates radial tension and tangential compression in glass. Polymer helps alleviate stresses at both temperature extremes. The contour plot of 1st principal stress at 150^{o}C is shown in Figure 5.56 along with the change of stress with respect to radial distance. There is no stress in y-direction on TPV surface due to free boundary. The stress in copper is mainly hoop stress due to expansion at high temperature. Therefore, 1st principal stress in copper is chosen as the metric to predict maximum tension in titania film covering the TPV surface. In previous section, by interpreting the Raman measurements, a stress around 52 MPa was estimated.



(a) **(b)**

Figure 5.56.(a) Contour plot of hoop stress (tangential, σ_z) in TPV and on top surface approximately at the region of Raman spectra collection in TPV and (b) variation of stress values on nodes at TPV surface with radial distance to TPV origin.

As seen in Figure 5.56, thermomechanical stress on TPV surface approximately around the measurement point shown in Fig.5.54.b varies in the range 47-51 MPa. The stress due to expansion of copper at point shown in Fig.5.56.a can be considered negligible due to fast decaying stresses with getting away from via center. Therefore, FEM results predict a stress difference of 49 MPa between 2 measurement points. Therefore, FEM results closely match the estimated stress based on Raman spectrum measurements, in spite of the assumptions and inaccuracy in the placement of laser beam spot for Raman measurements.

5.8 Summary

In this Chapter, reliability characterization of TPV was presented. As described in the previous chapters, various methods are available for TPV fabrication in glass. Test vehicles corresponding to each method were designed, fabricated and subjected to reliability tests. Reliability test vehicles consisted of daisy chain structures with four-point probe pads for DC resistance measurement, CPW transmission lines for RF s-parameter measurement and bond pads for IC assembly on both-sides. SEM imaging was conducted on sample cross-sections after reliability tests. Furthermore, a method to directly measure the stresses in glass and TPV were developed using anatase titania thin films. Based on test results, following conclusions were made:

- Strains induced during thermal cycling were not high enough to create major cracking in Cu, which explains the high number of cycles without any changes in resistance. This result agrees with high fatigue life of TPVs based on modeling results.
- Copper/Glass separation on glass surface and glass cracking at via corner and TPV pad edge were frequently observed in bare glass samples, which explain the necessity of having a thin polymer layer on glass surfaces to improve adhesion of copper on the interposer and control the stresses in the TPV corner by using smaller TPV diameter or copper thickness.
- Among polymer-laminated glass samples, glass cracking failures were only observed with UV laser-drilled TPVs. This was expected from modeling results, as the defect sizes with UV laser were much higher compared to other via formation methods.
- Failures in TPV were independent of glass thickness. Modeling study predicts that thickness of glass shouldn't have a major impact on thermomechanical stresses. This was

confirmed by testing TPVs formed with same method, but in glasses of different thicknesses.

- Raman measurements on anatase titania coatings were shown as a feasible method to assess stresses on glass and TPV. Measurement results matched well with stresses predicted by analytical equations and modeling results.

CHAPTER 6

RESEARCH SUMMARY AND FUTURE EXTENSIONS

High-density through-package-via (TPV) technology is a key building block for all high performance applications such as 2.5D interposers and 3D packages with assembly of components on both sides of TPVs. Such packages are currently being developed for several applications ranging from high-speed processors, integrated camera modules, RF and mm wave modules. Glass is emerging as the front-up substrate material for these applications. However, reliability of Cu-TPVs remains a major concern in realizing glass-based 2.5 and 3D interposers and packages. Glass is a brittle material that can fail at strains as low as 0.2%. Due to high CTE mismatch between Cu and glass, high thermal stresses can develop in the glass substrate surrounding TPVs. These stresses can be further amplified in the presence of defects on TPV walls and corners, and they can eventually lead to crack formation in glass. In addition, the large strain deformations in copper metallization can lead to fatigue failures during thermal loadings. The key focus of this research is to investigate reliability of copper-plated through-package-vias in glass interposers.

The objective of this research is to model and design copper-plated through-package-vias, leading to fabrication of test vehicles for characterization of defects and validation of models by demonstration of reliability through accelerated lifetime testing. Four fundamental challenges were defined, including: 1) Stress as a result of large CTE mismatch between materials, 2) design for both coarse and fine-pitch Cu TPV failures and double side assembly, 3) handling and processing of thin glass panels, 4) nature of defects and corresponding reliability. Accordingly, four research tasks were carried out to address the aforementioned challenges, involving: 1) mechanical modeling and design of TPVs in glass 2) fabrication of test vehicles for reliability

characterization 3) reliability characterization of TPVs and 4) analysis of failures. This chapter presents the summary of this study with key contributions and potential future extensions.

6.1 Research Summary

6.1.1 Mechanical modeling and design of TPVs in glass

- Analytical and finite element models were developed to analyze thermomechanical stresses in TPVs. Extensive parametric modeling of TPVs was performed to provide design guidelines for reliable TPVs.
- Parametric models suggested that decreasing via diameter leads to lower probability of failure if aspect ratio is kept constant, thus resulting in higher reliability of TPVs. Thermomechanical reliability is of higher concern for fully-plated TPVs with diameters larger than 100 µm. For larger TPVs, low-modulus polymer liner with adequate thickness of above 5 µm is required to reduce stresses on glass.
- If TPVs with small diameter is required for high density I/O, glass thickness should also be reduced to keep the aspect ratio of TPV lower than 3.
- Thickness of glass does not have big impact on thermomechanical stresses. Reducing the thickness of glass reduces the thermomechanical stresses but handling thin glass is an engineering challenge.
- Plastic strains in copper TPVs were found to be low, leading to approximately 10000 thermal cycles of fatigue life. Therefore, in a 3D package, first and second-level interconnections with higher plastic strains present higher failure risk compared to vertical TPV interconnections.

- Mechanical models were validated by analytical calculations and Micro Raman stress measurements.
- From a manufacturer's point of view, as long as TPV formation method does not create large defects (< 2 μm) and glass surface is laminated with a low-modulus polymer liner, TPV would be reliable. Conformal plating also significantly lowers probability of glass cracking and copper delamination.
- With lamination of TPV sidewall with polymer, tolerable defect sizes increase. Also polymer applies compressive stress on defects. Therefore, with such a via-in-via approach, TPVs would be extremely reliable.

6.1.2 Fabrication of test vehicles for reliability characterization

- Test-vehicles were designed and fabricated for characterizing TPVs formed with various TPV formation approaches, including excimer, UV, CO2 lasers, and electrical discharge.
- Three glass package structures were investigated: polymer-laminated glass, bare glass, TPVs with polymer-liner.
- Measurements were performed in both DC and RF domains for free-standing samples and after double-side assembly.
- Quality of TPVs formed with each of these methods were analyzed through cross-section SEM imaging to identify characteristic defect sizes and geometries corresponding to each method.
- Defects during via formation affect the occurrence of TPV failures. UV laser creates large surface defects compared to those from electrical discharge vias and laser-assisted chemical etching, thus increases probability of failure.

6.1.3. Reliability characterization of TPVs

- Reliability test vehicles with daisy chain structures and four-point probe pads were subjected to thermal cycling tests between -55°C and 125°C, and resistances of daisy chains were monitored throughout the test.
- Reliability characterization of fabricated test-vehicles suggests that the TPVs survive 8000 thermal cycles. For TPVs in polymer-laminated glass, SEM imaging confirmed no cracking in glass corners and good adhesion of polymer/glass the corners also suggested good adhesion at Cu/glass and Cu/polymer ad polymer/glass interfaces. Laser-based methods except UV laser and electrical discharge method creates small enough defects that do not lead to brittle fracture of glass. On the other hand, for TPVs in bare glass, cracks in glass were observed in stress concentration regions around lass corner and via pad edge.

6.1.4. Failure analysis and validation of models

- SEM imaging was carried out to observe the cross-section of the samples after thermal cycling.
- TPVs with larger diameter (>60 microns) and thicker copper (>25 microns) showed higher probability of glass cracking at the TPV corners, as also predicted by the models.
- Polymer stress buffer lining can help enable thicker copper structures and larger via diameters.
- Larger via diameters and large copper thicknesses result in copper delamination failures, which are more prevalent on bare glass surfaces than polymer-laminated glass surfaces.

- As glass is a good insulating material, even in case of glass cracking, electrical functionality of TPVs did not deteriorate. Therefore, monitoring of electrical parameters of TPV do not provide much information on reliability of TPVs.
- From a manufacturer's point of view, reliability characterization of TPV at fixed dimensions should be implemented by fully-filled plating of TPVs, thermal cycling and cross-sectioning. If no failures were observed with fully-filled TPV, then probability of failure in the conformal TPV is much lower. Also, reducing glass thickness will not increase failure probability. However, increasing the glass thickness will increase aspect ratio and stresses.

6.2 Key Contributions

a. First fundamental investigation of TPVs in glass interposers and packages:

- Mechanical modeling to provide design guidelines for realizing highly reliable TPVs in glass with various interposer structures
- Model-to-experimental validation of different failure modes such as glass cracking and copper delamination
- Design and demonstration of reliable TPVs in both DC and RF domains with both free-standing glass interposers and after die assembly.

b. Characterization of surface defects in TPVs from various formation approaches

c. Design guidelines for reliable TPVs in glass

d. Micro Raman piezo spectroscopy for direct stress measurements in glass using anatase Titania stress-sensor films

6.3 Future Extensions

The basic models and methodologies established in this thesis can be further extended to other areas of package reliability. Four of them are highlighted here:

Impact of TPV defects on RF performance: Recent feedback from end-users indicates that RF performance is sensitive to surface roughness and interfacial micro cracks, although measurable degradation in DC performance is not seen. This effect is expected to be more significant for mm wave applications. Specialized test-structures are required to de-embed the effect of TPV wall roughness and defect growth on mm wave performance.

High-power embedded ICs with thick copper structures: Glass is an excellent high-temperature packaging material. However, large conductor structures are needed to package high-power devices that can create hot spots inside the glass, leading to local CTE mismatch and failures. These structures can include copper through-vias, copper slugs or bonded heat-spreaders. Copper is an outstanding electrical and thermal conductor. However, it induces thermo mechanical stresses in glass. Detailed thermal and thermomechanical models need to be developed to design large conductors in glass with low stress.

Model validation through direct-stress measurement: Micro Raman piezospectroscopy can directly measure stresses in glass with micron-level spatial resolution. The use of Raman-active anatase films as stress sensors in glass, thus, provides unique opportunities to study reliability of glass. If the anatase film is deposited as a TPV liner, the interfacial stresses can be measured by

probing the titania regions on glass TPV walls with the Raman technique. Stress maps in glass can be experimentally obtained and validated with FEM predictions.

Reliability in high-temperature packages: The design and reliability models presented here can be extended to study TPV and overall package reliability in high-temperature packages. This requires extensive characterization of material properties as a function of temperature and degradation of properties with time, temperature, and humidity. The stress-free temperatures for various materials also need to be accurately determined because they have a strong impact on the model predictions.

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